GENERAL EXERCISES

6.1 Explain why two registers are needed rather than a single edge-triggered register to make a DAC function with a μP and also in flow-through mode.

6.2 The binary-weighted DAC of Fig. 6-4 has a maximum output voltage of +10 V. If $R_F = 40\ k\Omega$ and $V_B = -4$ V, select values of R_3, R_2, R_1, and R_0 to achieve the maximum possible conversion factor.

6.3 Repeat problem 6.2 for a 6-bit DAC. In this case, find values of R_5, R_4, R_3, R_2, R_1, and R_0. What is the CF in this circuit?

6.4 In Fig. 6-5, assume that $R_F = 4\ k\Omega$, $R_0 = 20\ k\Omega$, and $V_{REF} = 8$ V. What is V_A for an input code of 1010?

6.5 In problem 6.4, select R_F to create a conversion factor of 0.6 V.

6.6 The LSB resistor in a 6-bit binary-weighted DAC is 320 kΩ. What is the value of the MSB resistor? What is the change in absolute value of MSB resistance to cause a worst-case change in V_A of ±1/2 LSB?

6.7 The ladder DAC of Fig. 6-6(a) has $R_F = 20\ k\Omega$, $V_{REF} = -12$ V, and is an 8-bit DAC. Calculate R to result in $CF = 0.04$ V. Calculate the output voltage for an input code of 10011101.

6.8 If the conversion factor of an 8-bit ladder DAC is 0.04 V and $V_{REF} = -12$ V, calculate the change in V_{REF} to cause a ±1/2 LSB change in V_A.

6.9 If $R_F = 20\ k\Omega$ and $R = 20\ k\Omega$, select V_{REF} to give a $CF = 0.8$ V in the circuit of Fig. 6-10.

6.10 Suppose one has an 8-bit converter and a 7-bit converter. The analog output ranges of both converters are 0–10 V. What is the LSB value of each converter? Now explain how applying 7 bits to the 8-bit converter (LSB of the 8-bit converter unused) results in the same quantum interval as the original 7-bit converter.

6.11 Derive Eq. (6-12) for the BCD DAC. Show that Fig. 6-8 performs the correct conversion for the code 100101010111.