

Analog to Digital conversion

- A number of A/D converter types
- The one chosen depends on the application and on the performance

Types

- successive approximation
- Tracking A/D
- Dual slope A/D (integrating) least cost
- parallel A/D fastest
- Two stage parallel A/D

11.4 Analog-to-Digital Conversion

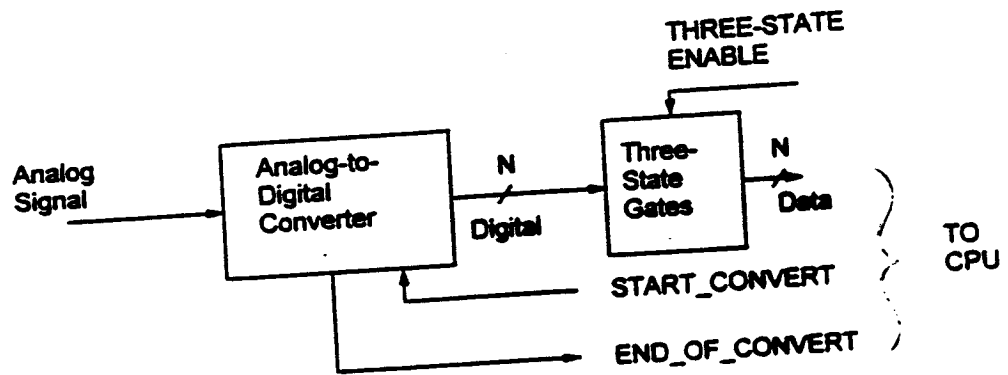


FIGURE 11-8 Analog-to-digital converter system. *Cuej*

Analog to Digital converters ADCs

① A/D converter Functions sampling, quantizing & encoding

② The mechanization of all A/D converters is by either

- ① integrating method
- ② voltage comparison method

method & speed

- integrating 0.45 to 1ms

- Voltage comparison
1ms to 10ns

Technique

Dual slope / charge balancing /
voltage to frequency

flash or parallel ✓
tracking ✓
successive approximation

} Conversion time

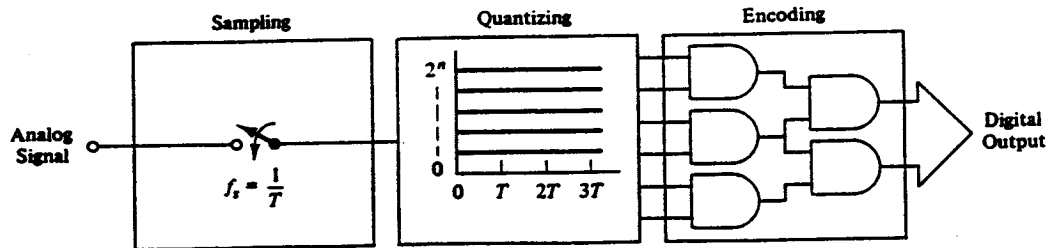


Figure 5-18. A/D Converter Functions

performance parameters

In order to select an ADC it is important to understand the definition of the converter specification & how they apply to the analog signal being converted.

A/D specifications

① Conversion Time

Time required to complete conversion of input signal

$$f_{\max} = \frac{1}{2 \times \text{conversion time}}$$

(imp) it establishes the upper signal frequency limit that can be sampled without aliasing

② Resolution

The number of bits in the converter gives the resolution (smallest analog input signal for which converter will ~~provide~~ produce a digital code

$$\text{Resolution} = \frac{\text{full scale signal}}{2^N}$$

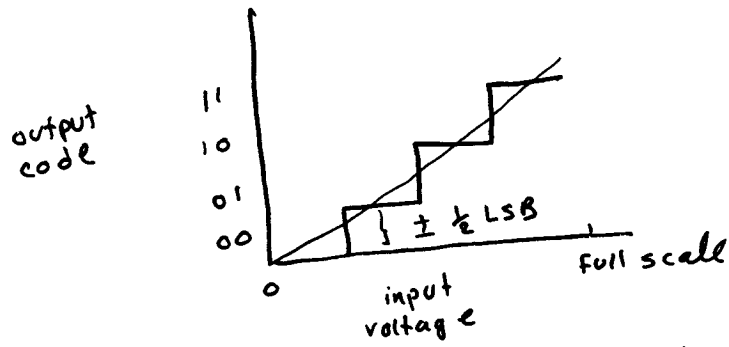
i.e 8 bit A/D & 5 volt full scale

$$\text{res} = \frac{5}{256} = 19.5 \text{ mV}$$

Others

Accuracy, linearity, Missing code, aperture time

③ Linearity: is the deviation in output codes from a straight line drawn through zero & full scale



the best that can be achieved is $\pm \frac{1}{2} \text{ LSB}$

④ Accuracy: quantization error in an ADC is generally $\pm \frac{1}{2}$

additional sources of error are

- linearity
- offset
- MUX

Total absolute error = \sum error sources

↳ typically $\pm 1 \text{ LSB}$

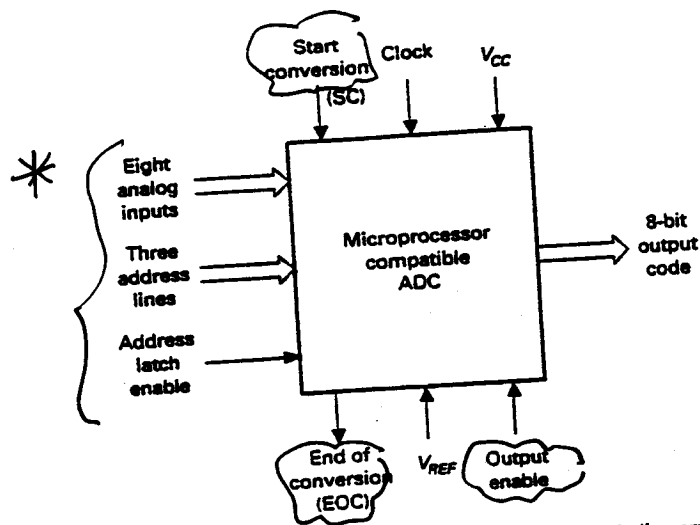


Figure 7-1 A microprocessor-compatible ADC block diagram.

ADC generally has two control lines that allow handshaking with external devices

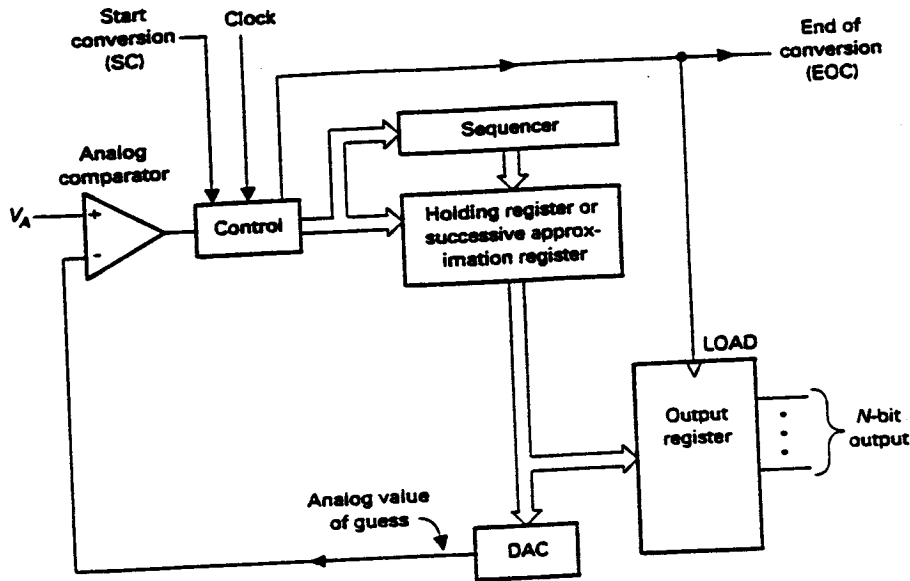
- start conversion
- end of conversion

(Note) In many cases an output enable line must be asserted to enable the digital code onto the up bus

* IF ADC is up compatible → it may also provide several multiplexed input channels

- address lines & address latch strobe to select the proper channel.

Successive approximation



most widely used A/D

Figure 7-4 Successive approximation ADC.

- is based on intelligent Trial-and-error method
i.e. number guessing with feedback

- operation
- First guess or approx
- ① when SC is asserted → control instructs the sequencer to place a '1' in MSB position of 'holding reg'
 - ② All other bits remain at 'zero level'
- * Each approximation can be checked in a clock period
thus N-bit conversion requires $\approx N$ clock periods

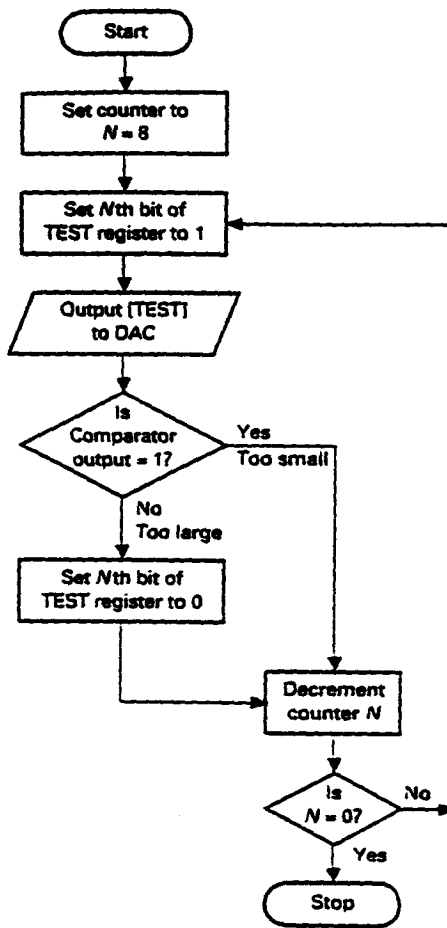


Figure 7-9 Flowchart for successive approximation ADC.

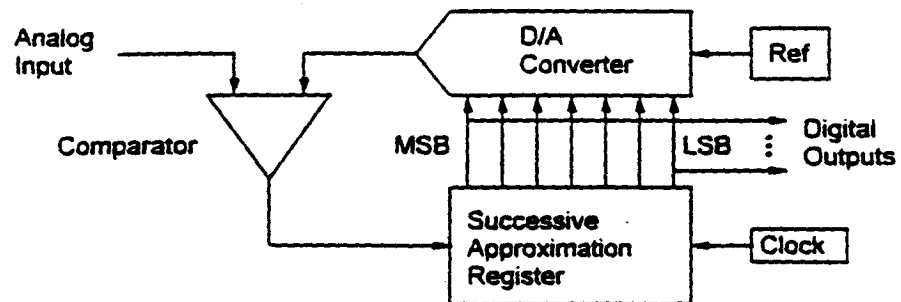


Figure 11-7 Successive approximation A/D.

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Example

6-bit A/D with range 0-5V

step size
 $\frac{5}{2^6} = 0.078$

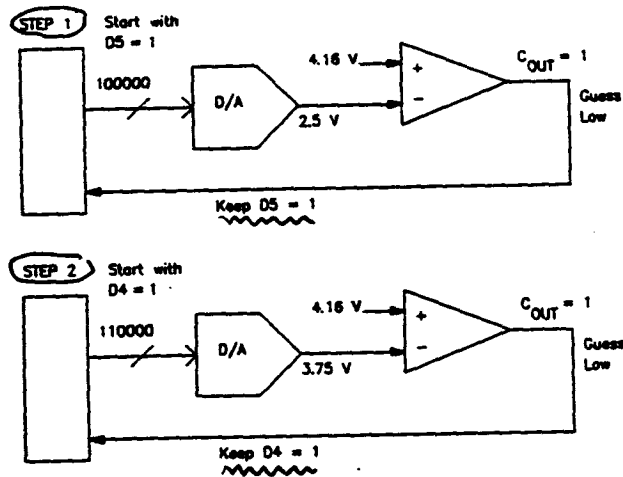


Figure 12.7 Successive-Approximation Example

(continued on next pa

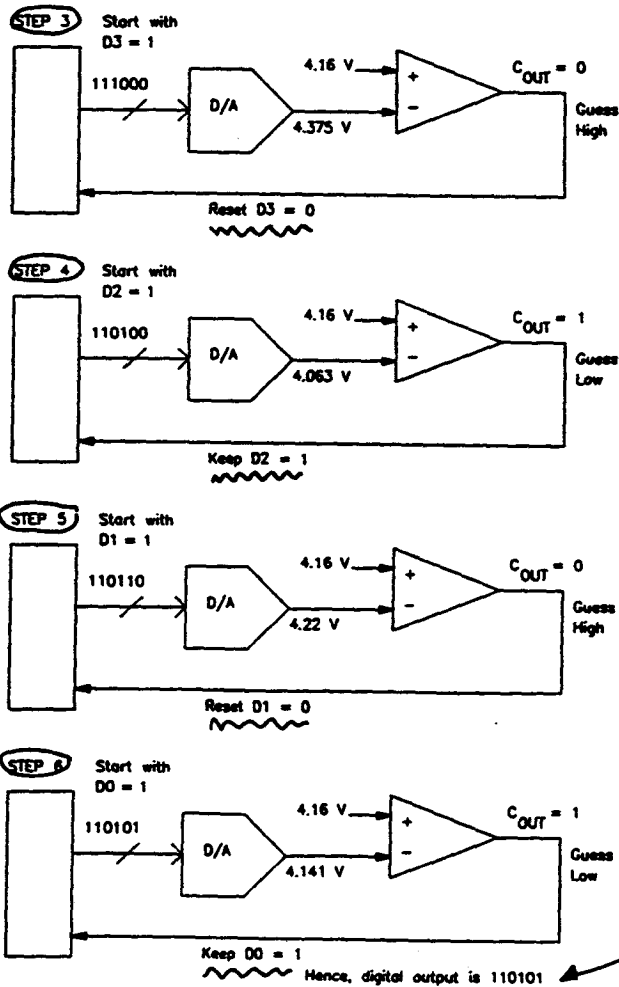


Figure 12.7 (continued)

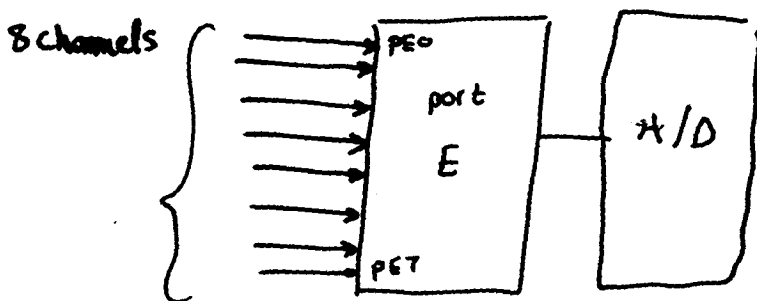
$4.16 - 4.141 =$
 0.019
 error is
 smaller
 than $\frac{1}{2}$ LSB

ADC's of Motorola μ computers

- 6811 / 6812 μ controllers have built in ADCs

Common features

- ① Eight - channel operation
- ② 8 - bit resolution
- ③ successive approximation conversion technique
- ④ Two operation modes:
 - ① single sequence of conversion , then stop
 - ② continuous conversion
- ⑤ Two channel selection modes
 - ① multiple conversion of a single channel (e.g channel 1,1,1,1)
 - ② One conversion each on a group of channels (e.g channels 0, 1, 2, 3)
- ⑥ external V_{RH} , V_{RL} analog high / low references



can operate in a single channel or multichannel

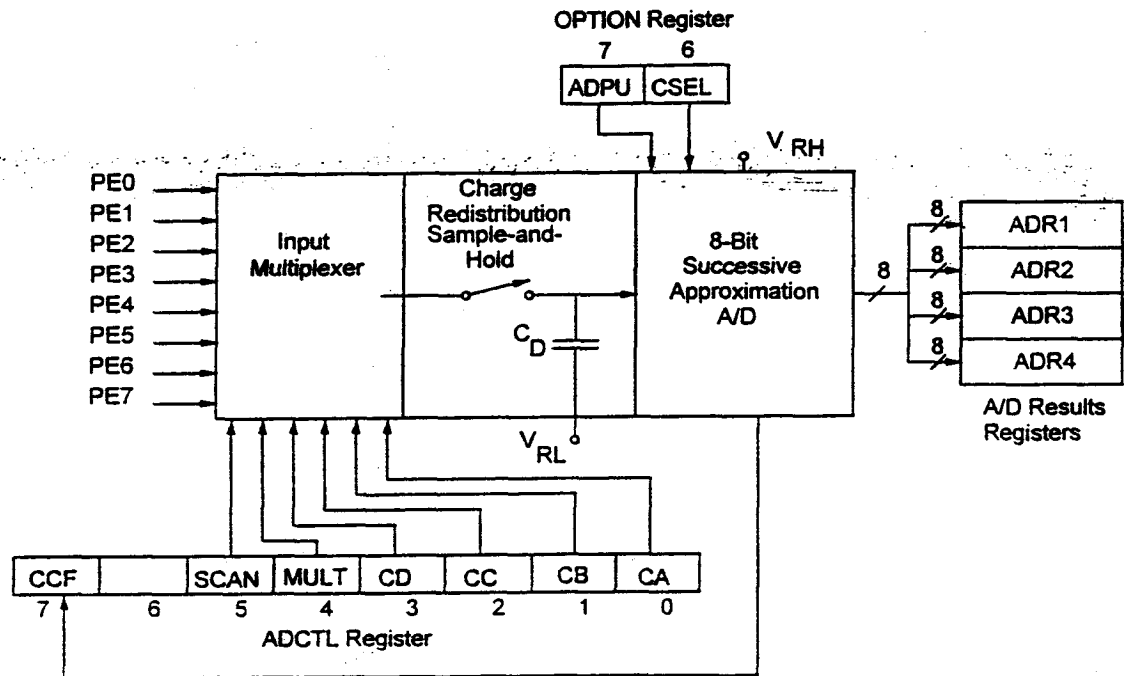
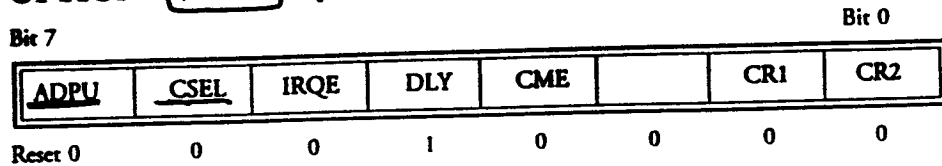


Figure 12-1 M68HC11 analog-to-digital converter block diagram.

the 6811 ADC system is enabled by setting ADPU = 1 in option Reg when ADPU = 0, port E operates as a normal digital input port

Chapter 12: M68HC11 Analog Input and Output

OPTION **\$1039** System Configuration Options



ADPU

A/D Power-up
 → 0 = A/D not powered-up (default).
 1 = A/D charge pump powered-up.

Setting the ADPU bit turns on a charge pump used for the analog switches in the multiplexer and the charge redistribution circuits. A delay of at least 100 μs is required to allow this process to stabilize.

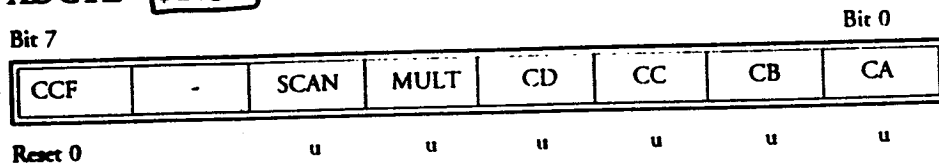
CSEL

Clock select.
 → 0 = select E-clock for the charge pump (default).
 1 = select on-chip RC oscillator.

CSEL also selects the clock source for the charge pump used when programming the EEPROM. Table 12-1 shows how to choose CSEL for various E-clock frequencies.

The A/D Control/Status Register contains the conversion complete flag, CCF, and bits to control the multiplexer and the channel scanning.

ADCTL **\$1030** A/D Control/Status Register



CCF

0: Conversion in progress
 1: conversion complete

TABLE 12-1 CSEL for various E-clock frequencies

E-Clock frequency	CSEL for A/D operations	CSEL for EEPROM programming
≥ 2 MHz	0	0
750 kHz - 2 MHz	0 to achieve the highest A/D accuracy	1 for EEPROM programming efficiency
< 750 kHz	1	1

SCAN: continuous scan control
 0: single sequence of conversion
 1: continuous conversion

Mult:

0: sequence of conversions on a single channel.
 1: sequence of conversions on multiple channels

- \$1031 ADR1
- \$1032 ADR2
- \$1033 ADR3
- \$1034 ADR4

A/D performs 4 conversions requiring 32 cycles

Single channel operation if software clears bit Mult = 0
 subsystem operates in single channel mode.
 (i.e. only one channel is used and its results placed in all four result registers when conversion is complete)

in
 ADCTL
 \$1030

TABLE 12-2 Single-channel conversion table, MULT = 0

CD	CC	CB	CA	Channel converted
0	0	0	0	PE0
0	0	0	1	PE1
0	0	1	0	PE2
0	0	1	1	PE3
0	1	0	0	PE4 ¹
0	1	0	1	PE5
0	1	1	0	PE6
0	1	1	1	PE7

channel select
 bit settings that
 determine which
 channel has its input
 converted to digital.

TABLE 12-3 Multiple-channel operation, MULT = 1

CD	CC	CB	CA	A/D result registers			
				ADR1	ADR2	ADR3	ADR4
0	0	X	X	PE0	PE1	PE2	PE3
0	1	X	X	PE4	PE5	PE6	PE7

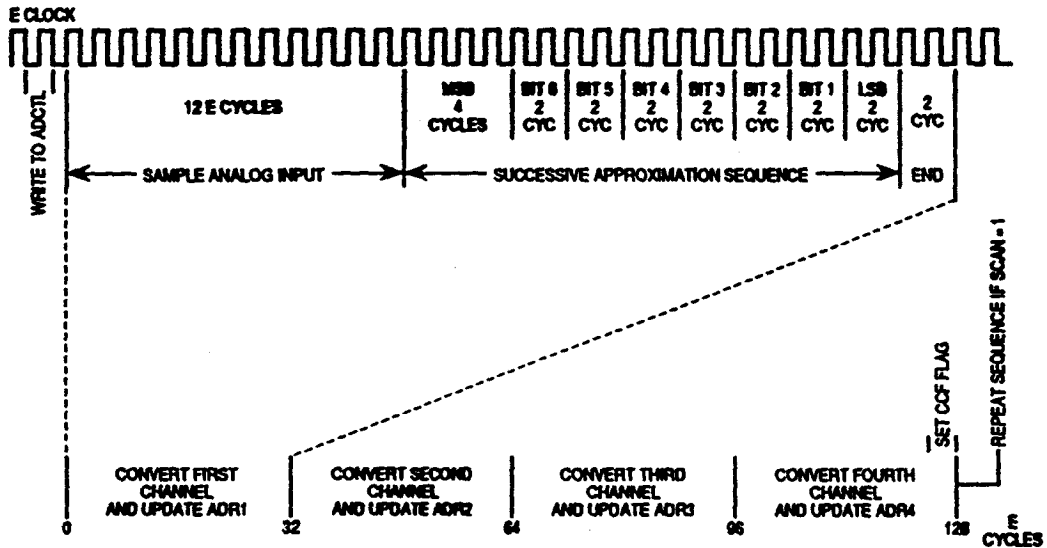


Figure 12-2 Timing diagram for a sequence of four A/D conversions (reprinted with permission of Motorola).

¹ PE4-PE7 are not available in versions of the M68HC11 in the 48-pin package.

How to operate ADC

Note polling
no interrupt available

Initialization

Turn on ADC
wait 100µs
rts

sampling

choose setting for ADCTL
CCF; SCAN, MULT
choose a channel
CD, CC, CB, CA
store in ADCTL
continuously check CCF
load result from Register
RTS

Note CCF flag is cleared automatically
every time (any) data is written to
register ADCTL

Imp if scan = 0 you have to initiate a conversion
each time by writing to ADCTL

Using Nyquist theory to determine sampling rate

(imp) There are two errors introduced by the sampling process

- ① Voltage quantizing \rightsquigarrow due to finite word size of ADC
- ② Time quantizing is caused by the finite discrete sampling interval

Nyquist theory states that if the signal is sampled at f_s , then the digital samples only contain frequency components from 0 to $0.5 f_s$ (i.e. if analog signal does contain frequency components larger than $0.5 f_s$ then there will be an aliasing error).

aliasing is when the digital signal appears to have a different frequency than the original analog signal.

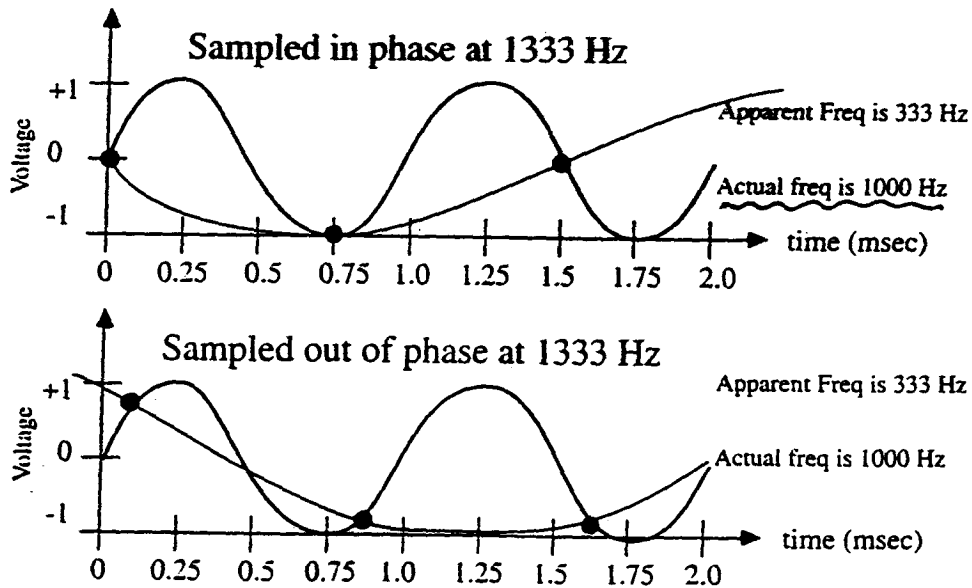
Simply put

if one samples a sine wave at a rate f_s $v(t) = A \sin(2\pi ft + \phi)$

Q is it possible to determine A, f, ϕ from digital samples?

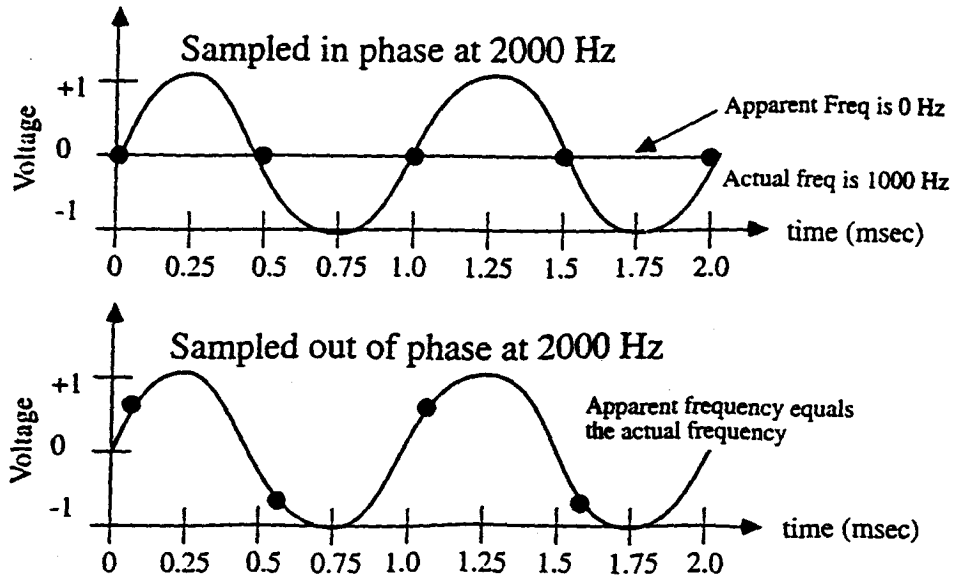
Figure 12.22
Aliasing makes the 1000-Hz signal appear as a 333-Hz signal.

Nyquist theorem
 $f_s > 2f$
yes



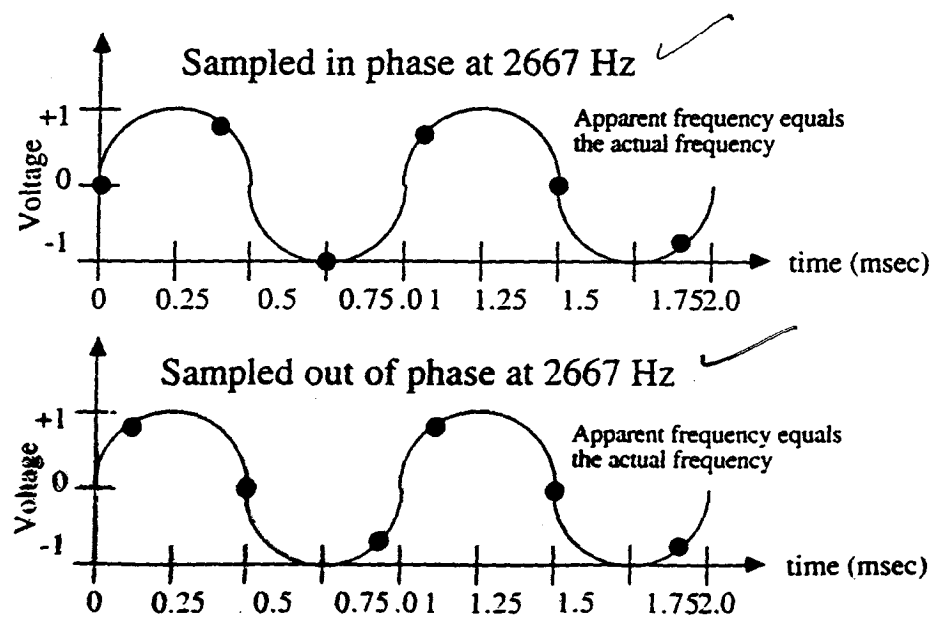
If 1000 Hz sine wave is sampled in phase at 2000 Hz then the digital samples appear as a constant (0 Hz)

Figure 12.23
Right at the Nyquist frequency aliasing may or may not occur.



Imp When the sampling frequency is exactly equal to twice the input frequency, the aliasing error is dependent on the phase between the signal and ADC sampling

Figure 12.24
Aliasing does not occur when the sampling rate is more than twice the signal frequency.



The choice of sampling rate f_s is determined by the maximum useful frequency contained in the signal.

One must sample at least twice this max useful frequency

Figure 12.25
Aliasing does not occur when the sampling rate is more than twice the signal frequency.

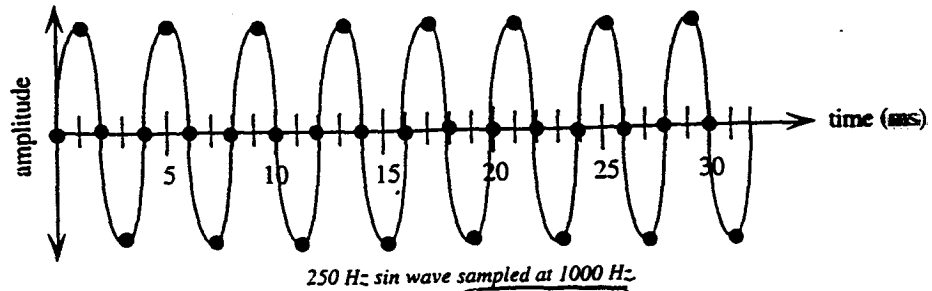


Figure 12.26
Right at the Nyquist frequency aliasing may or may not occur.

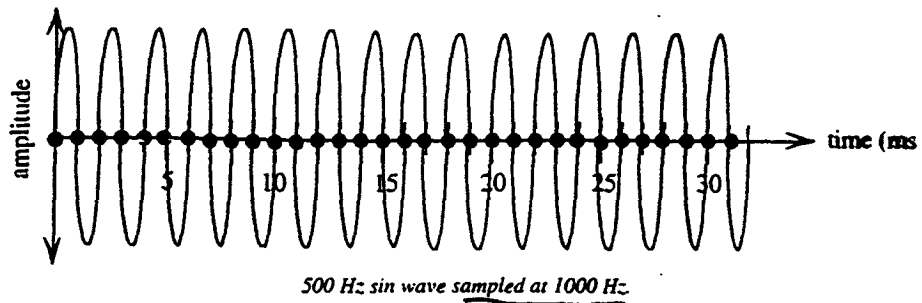


Figure 12.27
Aliasing makes the 533-Hz signal appear as a 33-Hz signal.

