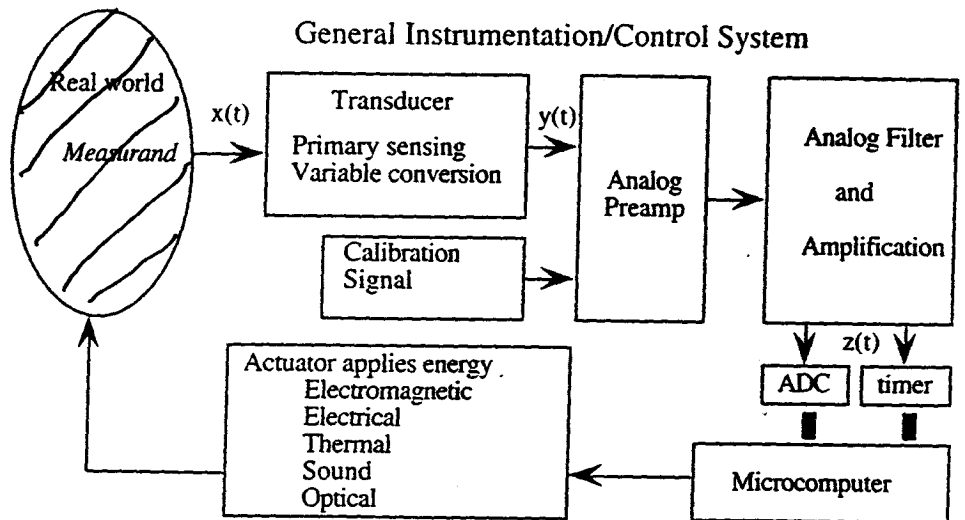


Data Acquisition systems

purpose understand general concept of acquiring analog signals (or acquisition of physical data) in a form that can be used (manipulated) by a digital computer

Digital? - DSP / data storage / high noise immunity - ...

Figure 12.2 Signal paths of a DAS.



- * Type of Transducers (sensors)
- * signal conditioning
- * concept of A/D D/A S/H (Types)
- * understand system errors (analysis)
- * Applications.

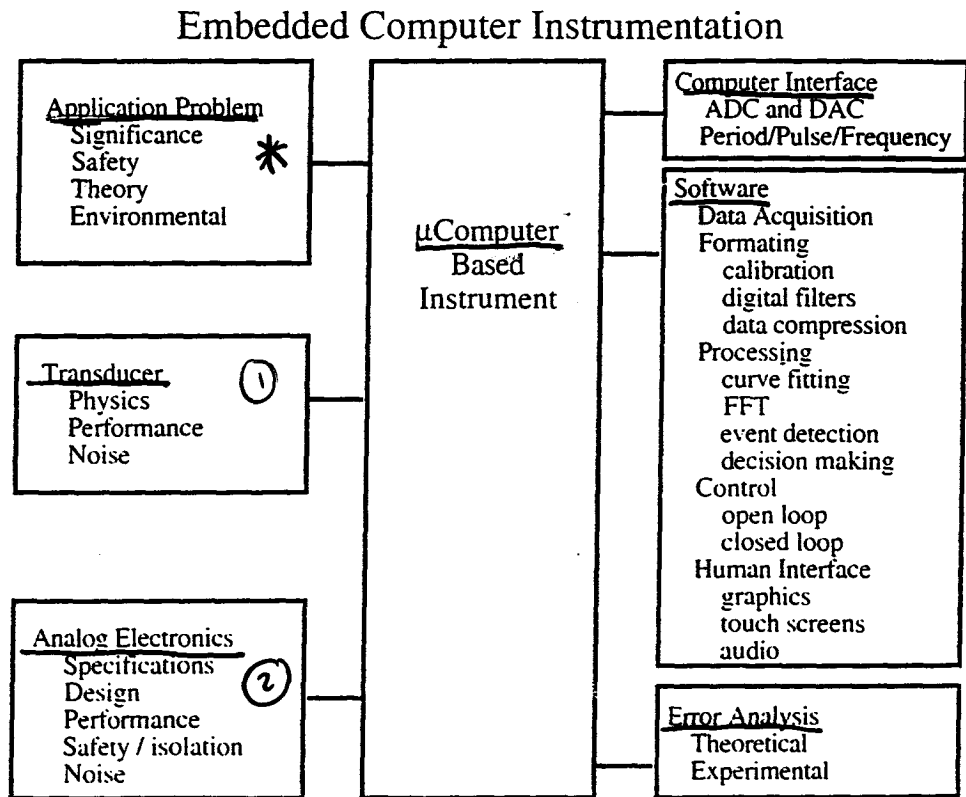
A complete Data Acquisition system

- Application problem
- Transducer
- Analog electronics

- μ computer
- A/D D/A
- software

error analysis

Figure 12.1 Individual components are integrated into a DAS.



DATA ACQUISITION & CONVERSION

① Recieve analog info from physical processes
→ Use transducer (sensor) to convert these variable processes to electrical signals (voltage or current) i.e. Thermocouple Temp → voltage

② signal conditioning:

① isolation & buffering: protection from dangerous voltages

② Amplification: need full scale signal for conversion

③ Bandwidth limiting: i.e. low pass filter to limit range

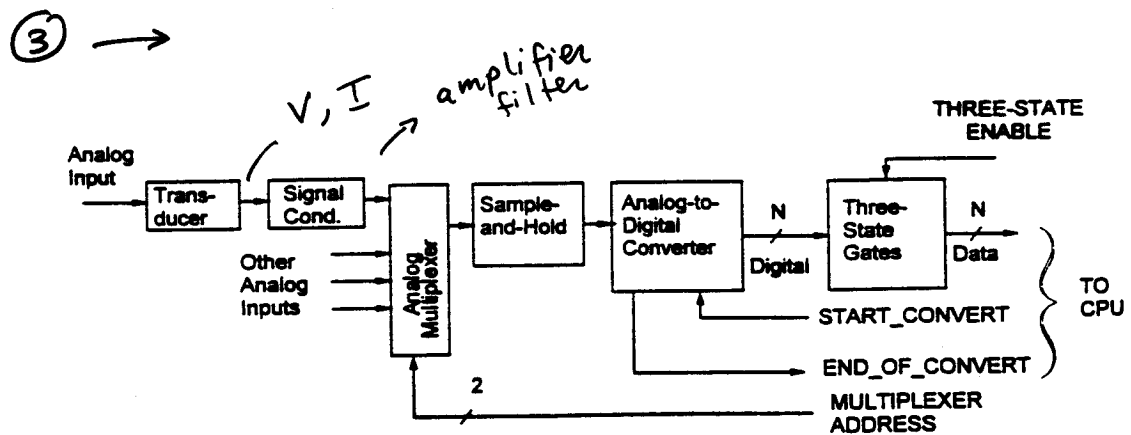


Figure 11-1 Data acquisition system.
2007

Concepts & Terminology

- Analog signals have a ratiometric range.
- These range from a low value to a high value

$0V$ to $5V$
 $-2.5V$ to $+12.5V$
 $4mA$ to $20mA$

Binary code representation

i.e. $00\$$ \rightarrow $0V$

$FF\$$ \rightarrow $5V$

$80\$$ \rightarrow $2.5V$

middle of analog range

if the analog range starts from a nonzero minimum value it is usually represented by an "offset binary code"

e.g. $-2.5V$ \leftrightarrow $+12.5V$
 \downarrow \downarrow
 $00\$$

Definitions

offset \rightarrow Minimum analog value

span \rightarrow Max to Min analog value

weight \rightarrow The analog change corresponding to a change in a bit in the digital number

of bits \leftarrow stepsize \rightarrow $\frac{\text{span}}{2^n}$

Resolution \rightarrow same as stepsize { smallest analog change resulting from changing one bit in digital

Equations

Conversion

analog number = (digital number x step size) + offset

digital number = (analog number - offset) / step size

≈ ((analog number - offset) / span) x 2^n

Example

analog range -5V → +5V

digital range is 8 bits

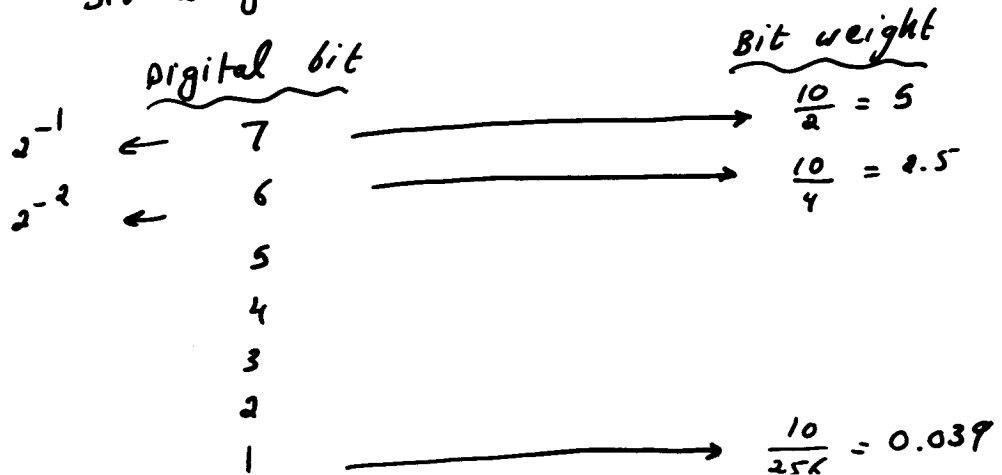
offset = -5V

span = 5 - (-5V) = 10V

step size = 10V / 2^8 = 10 / 256 = 39.1 mV = resolution

% Resolution = 1 / 256 x 100% = 0.391%

Bit weights for -5 to +5V



recall

eqn 12.1

$$\text{analog number} = (\text{digital number} \times \text{step size}) + \text{offset}$$



shortcut

$$\text{eqn } \underline{\underline{12.3}} \quad \text{analog number} = (b_{n-1} \times 2^{-1} + b_{n-2} \times 2^{-2} + \dots + b_0 \times 2^{-n}) \times \text{span} + \text{offset}$$

Example A 6 bit D/A has an analog output range of -2.5 to 5.0V. Calculate the analog output when input is % 010101 (decimal 21)

①

$$\text{offset} = -2.5 \text{ V}$$

$$\text{span} = 5.0 - (-2.5) = 7.5 \text{ V}$$

$$\text{step size} = \frac{7.5}{2^6} = 0.1172 \text{ V}$$

using 12.1

$$\begin{aligned} \text{analog number} &= 21 \times 0.1172 \text{ V} - 2.5 \text{ V} \\ &= -0.039 \text{ V} \end{aligned}$$

using 12.3

$$\text{analog number} = \left(0 \times \frac{1}{2} + 1 \times \frac{1}{4} + 0 \times \frac{1}{8} + 1 \times \frac{1}{16} + 0 \times \frac{1}{32} + 1 \times \frac{1}{64} \right) \times 7.5 + (-2.5 \text{ V})$$

$$= 1.875 + 0.469 + 0.117 - 2.5 \text{ V}$$

$$= -0.039 \text{ V}$$

-5V to +5V analog Range

Analog	Digital
-5	00
-3.75	20
⋮	
0	80
1.25	A0
$5 - 0.0391 = 4.961$	F5

Outside The Range

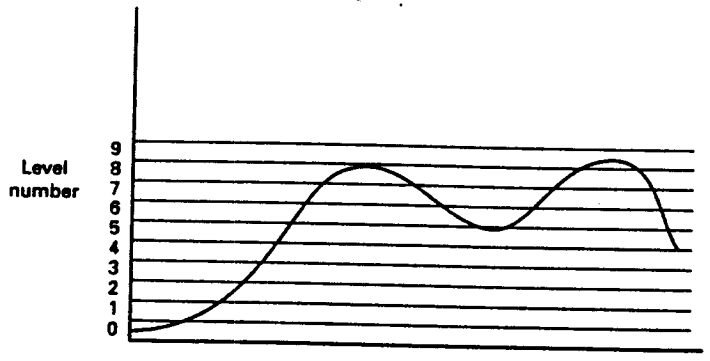
if input of an A/D is below the minimum or above the maximum of the range, the corresponding digital value will be min or max

i.e. 8-bit A/D with range of 0 to 5V has an input of -0.5V \rightarrow digital output will be 00

Variable step size

i.e. not all systems use uniform step sizes. pulse code Modulation PCM is used in telecommunication systems. since noise is more of a problem when the signal is weak, the step size is reduced for smaller signal amplitudes and is increased for larger amplitudes (i.e. step size \propto signal amplitude)

Quantum Interval & Error



An analog voltage quantized into equal width intervals.

Figure 5-1 Quantization levels of an analog signal.

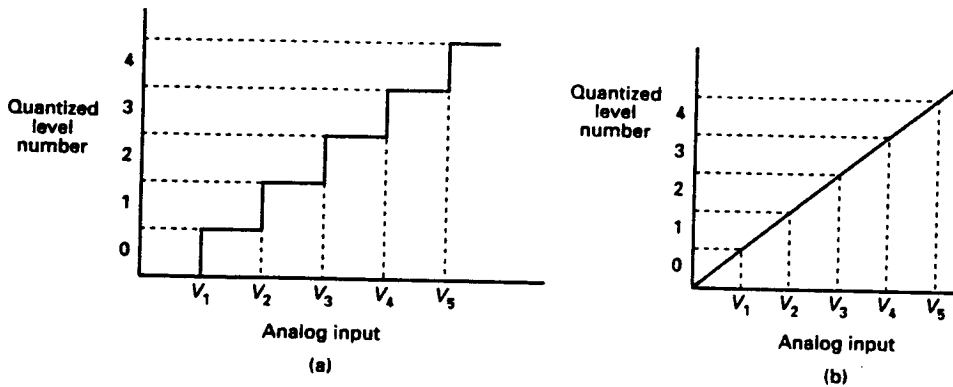


Figure 5-2 Analog input versus level number.

- A finite length digital code can represent only a finite number of levels

BUT an analog signal has an infinite number of values

* when an analog signal is to be represented by a digital code \Rightarrow the range of analog signal is divided into levels (quantization)

Figure 5-2

input	level
$0 - V_1$	0
$V_1 - V_2$	1
$V_2 - V_3$	2

"width of a level = q (quantum interval)

$$q = \text{LSB} = V_1$$

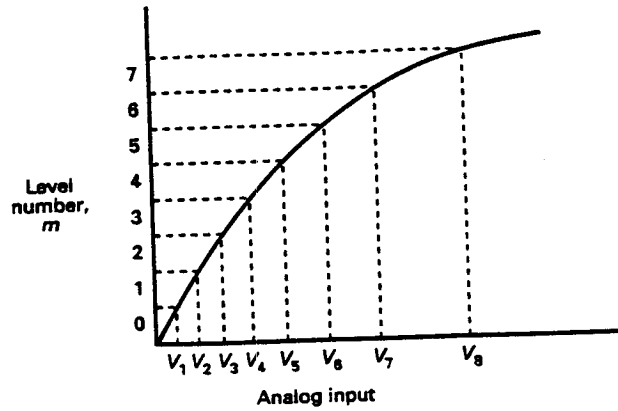


Figure 5-3 Variable quantum interval.

" We might have a variable quantum interval "

① In converting the analog signal to a digital code the digital code may simply represent the level at which the analog signal exists.

② IF a conversion is made at a time when the analog signal resides between levels 3-4 the output digital code should represent the number 3 !!

The use of a level number to represent the analog signals leads to an inaccuracy we call Quantization Error

Analog input vs error

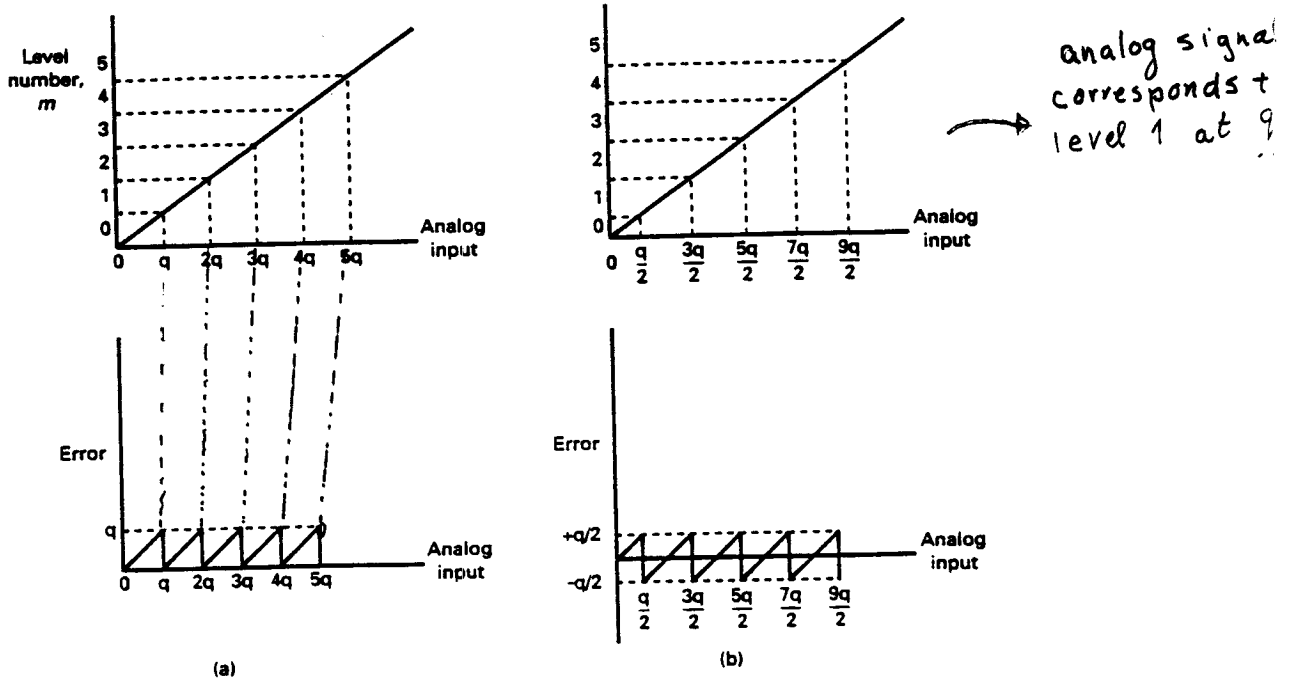


Figure 5-4 Analog input versus error. (a) Quantization error for equal quantum intervals. (b) Quantization error for first interval of $q/2$ or $1/2$ LSB.

- The error is calculated as the difference between the actual analog signal and the value represented by the level number

(a) error increases from 0 to q as the analog signal ranges from 0 to q
 "Greatest possible error = q "

(b) The first quantum interval is reduced to $q/2$ or $1/2$ LSB (while all other intervals remain at a value of q).

* since level '1' represents a value of ' q ' the error at this point is $-q/2$.

* error ranges from $+q/2$ to $-q/2$

max absolute error = $\boxed{q/2}$

Span of an Analog signal

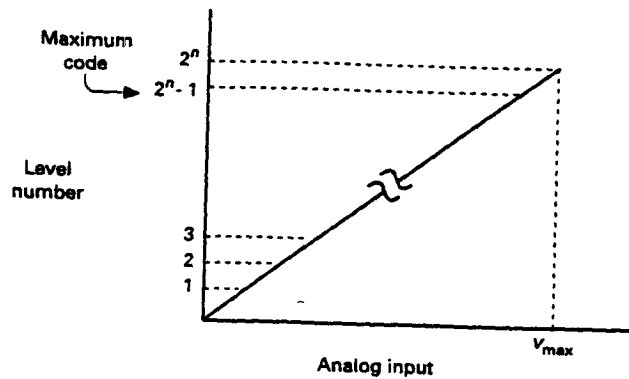


Figure 5-5 Output code as a function of analog input.

The span of the analog signal (to be converted) is defined in terms of the minimum & maximum values of this signal

* Assume signal span is extended from 0 - V_{max}

minimum quantum interval is calculated to be:

$$q = \frac{V_{max}}{2^N}$$

imp

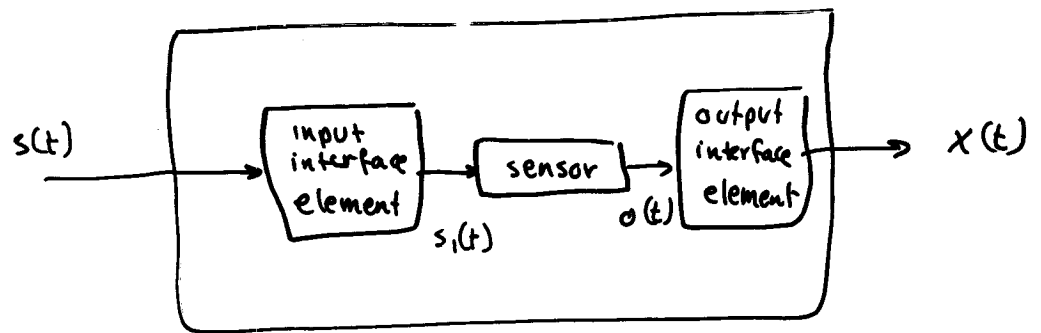
quantum interval & thus quantization error can be minimized by increasing N

limitations?

- ① Max # of bits may be limited by the computer that follows converter.
- ② The lower limit on the quantization error is influenced by the transducer & conditioning errors.

Transducer Def

The heart
of the
transducer
is the
sensor



Most comprehensive def

: any unit that
appears between any
two or more signals

More restricted

: is a unit that has
a physical variable as an input &
some analog **output** such as voltage
change, current

* input interface element has 3 primary functions

- ① provide improved coupling between measurand $s(t)$ and sensor
(matching function)
- ② protect the sensor from undesirable environmental effects
i.e coating to protect resistance temperature devices
- ③ convert $s(t)$ to another physical variable $s_i(t)$
required by a sensor that cannot respond to $s(t)$ directly

Sensors

position : potentiometer

Linear variable displacement transformer (LVDT)

Force : strain gauge
piezoelectric device

Temp : Thermistor
Thermo couple

Light Intensity : photoconductive cell
photo transistor

current : current transformer

(imp) often, other physical quantities are measured using variations of the sensors listed above.

i.e flow can be measured using force or temperature

* pressure is the amount of force per unit area, (So) flow rate can be determined by measuring the pressure drop across an element

or * measure the amount of heat removed from a heated element by the fluid

FIGURE 12-1 Some Common Sensors

position

outputs the angular position of the shaft

$$V = I \times R$$

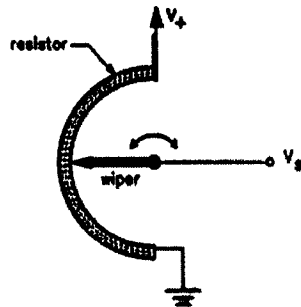
Force

strain gauge is a resistor whose resistance varies with the amount of stretching.

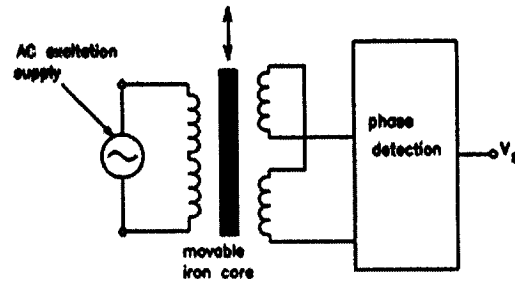
temperature

output a voltage that is related to temp at the tip of the probe

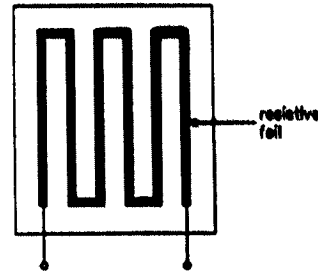
(works on principle of Seebeck effect)



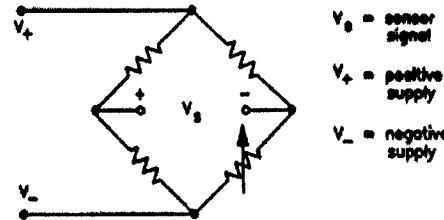
(a) Potentiometer



(b) Linear Variable Displacement Transformer LVDT



(c) Strain Gauge Pad

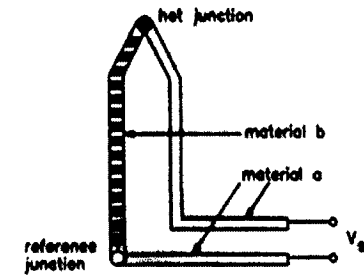


(d) Strain Gauge Circuit

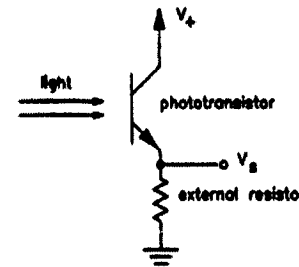
V_s = sensor signal
 V_+ = positive supply
 V_- = negative supply

- Transformer has primary & secondary winding
- voltage at secondary winding varies according to position of movable iron core.

change in resistance is detected by measuring the voltage change in wheatstone bridge ckt.



(e) Thermocouple



(f) Phototransistor

Light Intensity

acts like a variable current source.

(Note) relationship between voltage & temp is nonlinear

Figure 12.9
Potentiometer-based
position sensor.

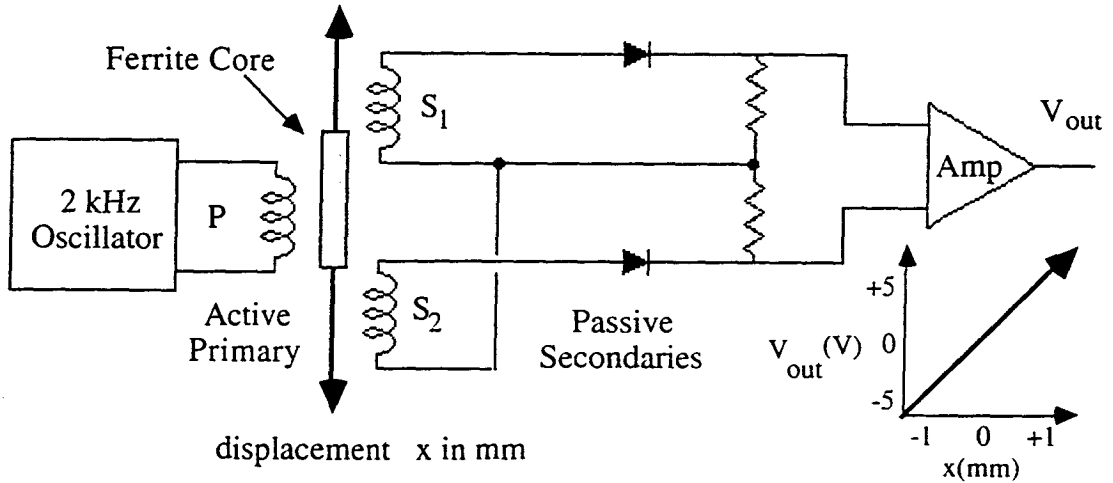
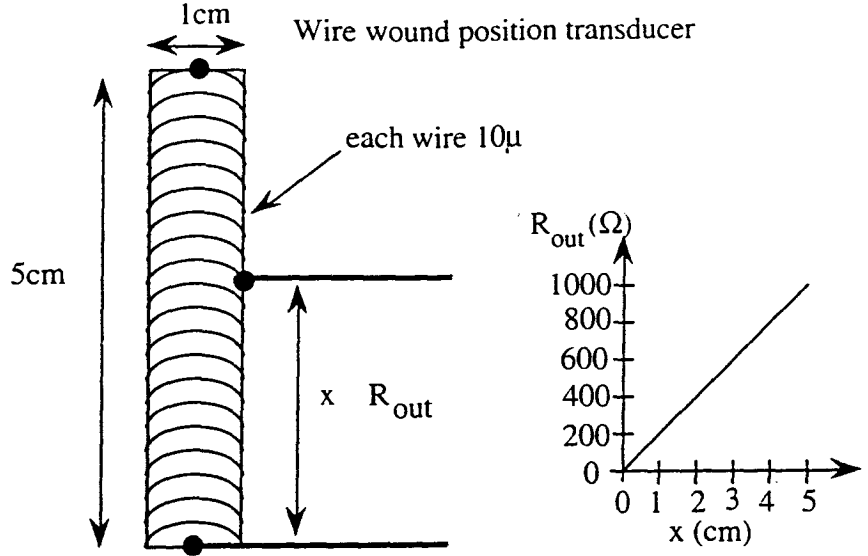


Figure 12.10 A LVDT measures displacement.

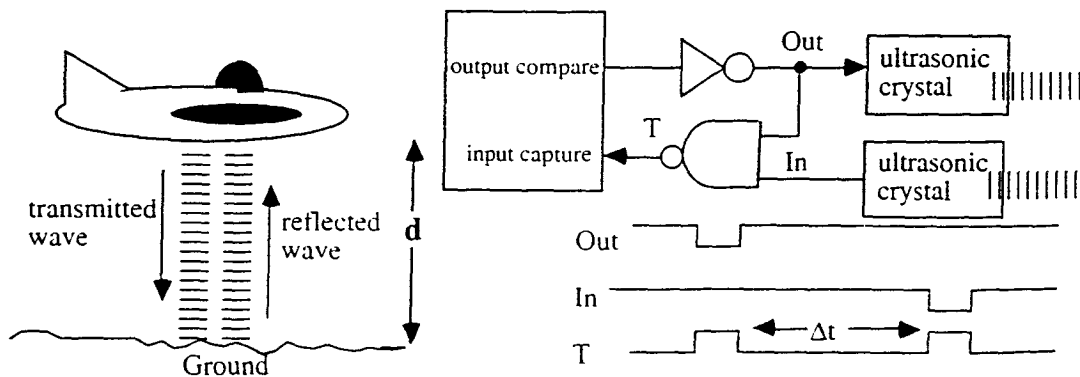


Figure 12.11 An ultrasonic pulse-echo transducer measures the distance to an object.

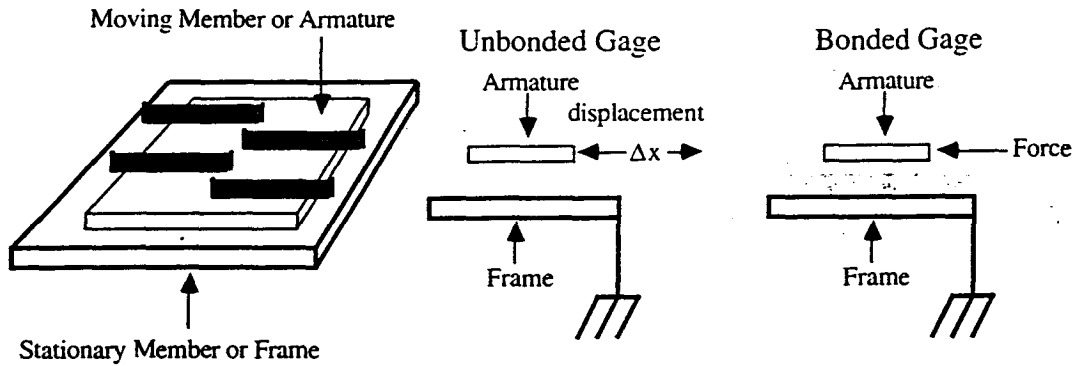


Figure 12.15 Strain gages used for displacement or force measurement.

The gage factor for an Advance strain gage is 2.1. The typical resistance R is 120Ω . If the gage is bonded onto a material with a spring characteristic

$$F = -kx$$

then the transducer can be used to measure force. The wires each have a significant temperature drift. When the four wires are placed into a bridge configuration, the temperature dependence cancels (Figure 12.16). A high-gain high-input impedance high-CMRR differential amplifier is required.

Figure 12.16 Four strain gages are placed in a bridge configuration.

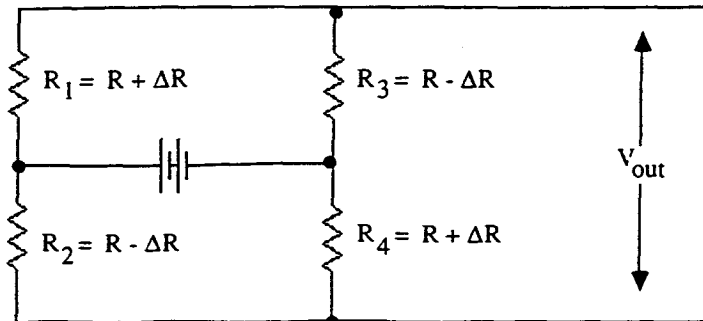
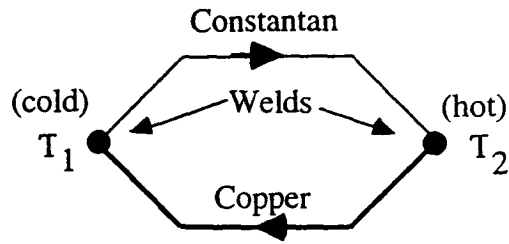


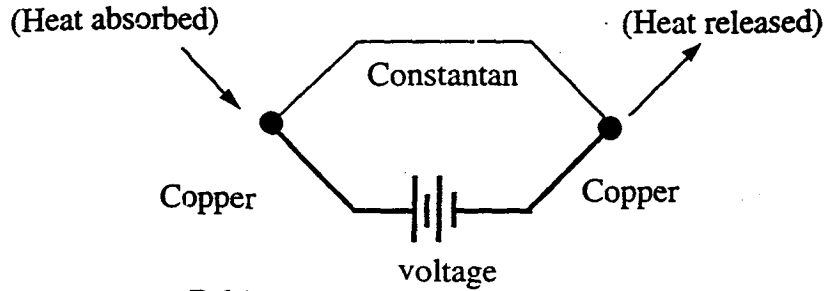
Figure 12.18
 When the two thermocouple junctions are at different temperatures, current will flow.



$$\text{current} = a (T_1 - T_2)$$

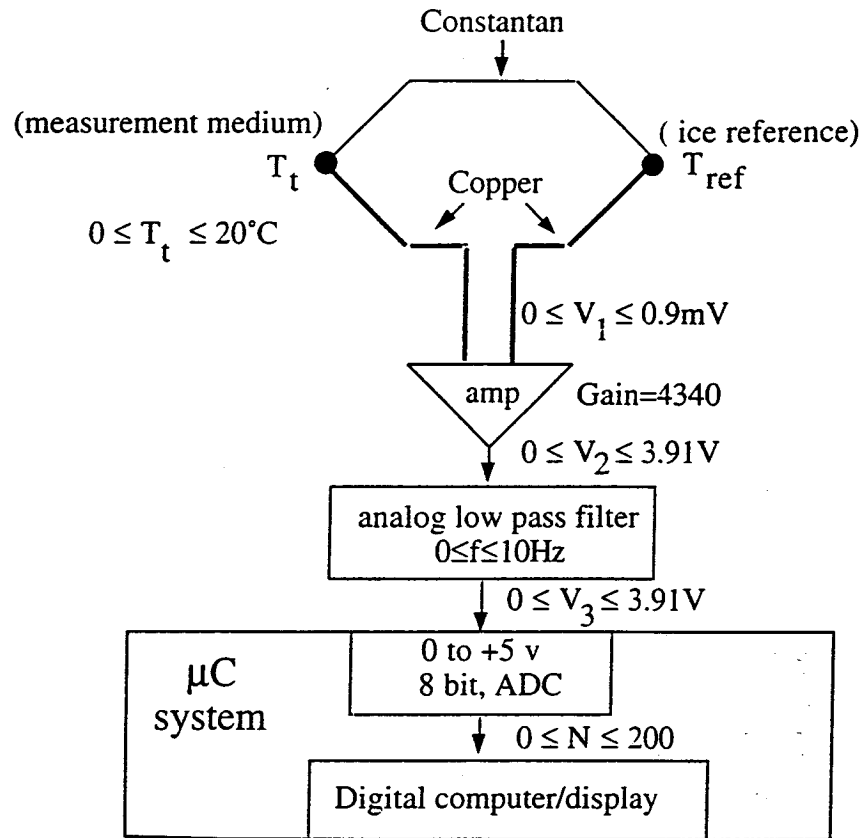
Seebeck effect = thermal to electrical

Figure 12.19
 When voltage is applied to two thermocouple junctions, heat will flow.



Peltier effect = electrical to thermal

Figure 12.20
An instrumentation and low-pass filter are used to interface a thermocouple.



Type—Thermocouple	$\mu\text{V}/^\circ\text{C}$ at 20°C	Useful range, $^\circ\text{C}$	Comments
T—Copper/constantan	45	-150 to +350	Moist environment
J—Iron/constantan	53	-150 to +1000	Reducing environment
K—Chromel/alumel	40	-200 to +1200	Oxidizing environment
E—Chromel/constantan	80	0 to +500	Most sensitive
R S—Platinum/platinum-rhodium	6.5	0 to +1500	Corrosive environment
C—Tungsten/rhenium	12	0 to 2000	High temperature

Table 12.7 Temperature sensitivity and range of various thermocouples.

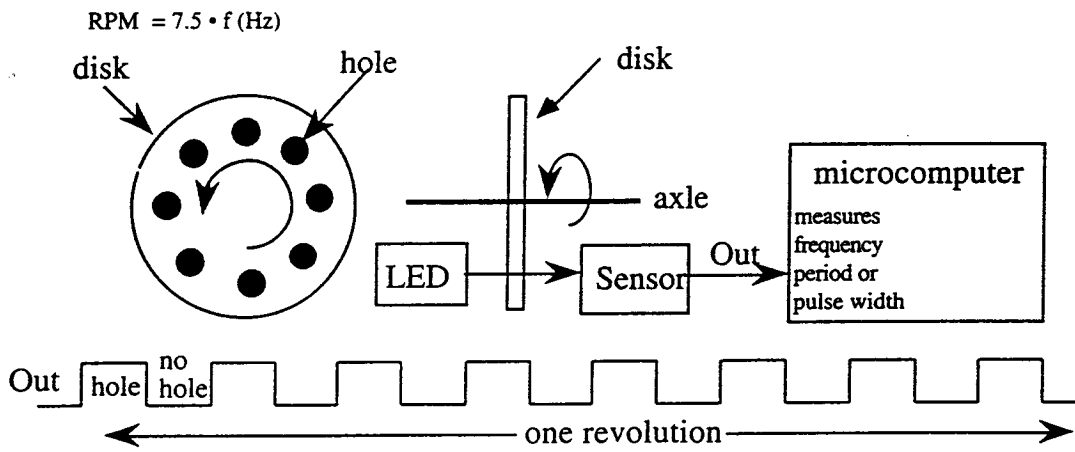


Figure 12.12 A LED-photosensor pair measures shaft rotation.

measuring the f

Figure 12.17
Thermistors come in many shapes and sizes.

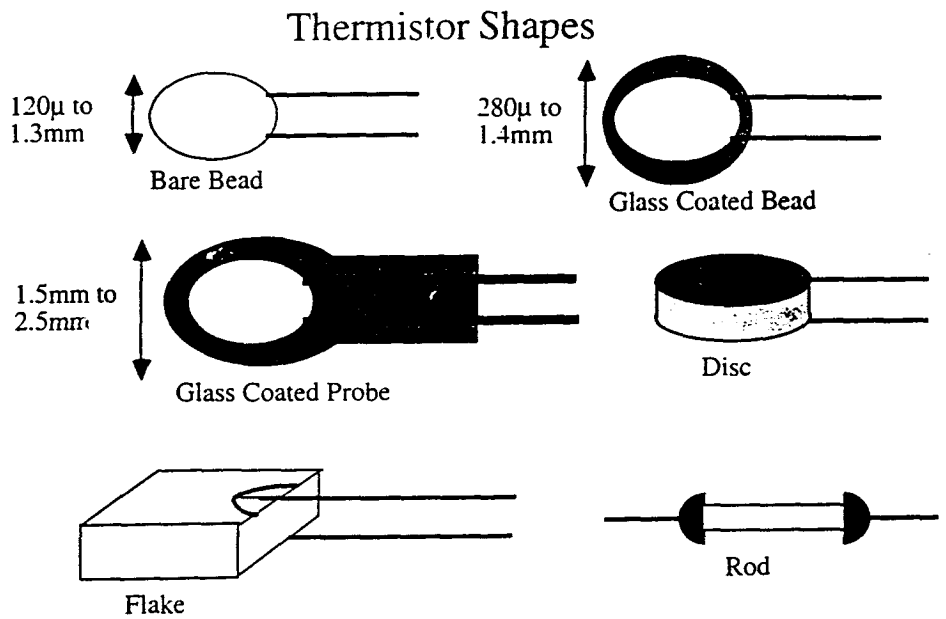


Table 12.6
Trade-offs between thermistors and thermocouples.

Thermistors	Thermocouples
More sensitive	More sturdy
Better temperature resolution	Faster response
Less susceptible to noise	Inert, interchangeable V versus T curves
Less thermal perturbation	Requires less frequent calibration
Does not require a reference	More linear

Signal Conditioning

(IMP) Raw sensor outputs are not always suitable for A/D conversion

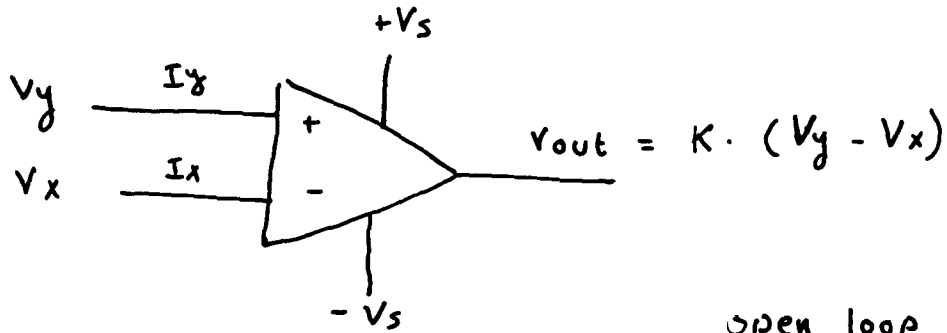
- signal conditioning circuits typically amplify the raw signal from a sensor. (i.e. thermocouple)
- signal conditioning also provide buffering so that the sensor signal is not affected by anything else connected to the ckt (i.e. minimize loading high impedance input / low impedance output)



Most signal-conditioning circuits employ operational amplifiers.

OP AMPS

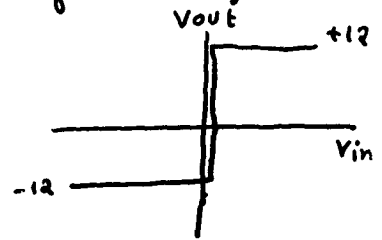
ideal op-Amp



open loop gain K

Rule #1

Voltage ranges are bounded by supply voltages i.e. $\pm 12V$



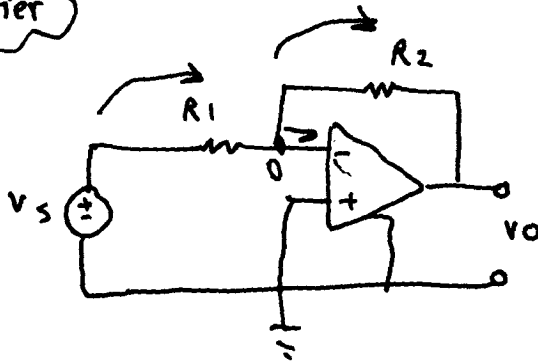
Rule #2 Input currents are zero because input impedance is large

Rule #3 Negative feedback drives $V_x = V_y$

$$V_{out} = K (V_y - V_x) \quad \text{since } K = \infty \quad V_y - V_x = 0$$

Rule #4 positive feedback or no feedback drives $V_{out} = \begin{matrix} -V_s \\ +V_s \end{matrix}$
i.e. saturation

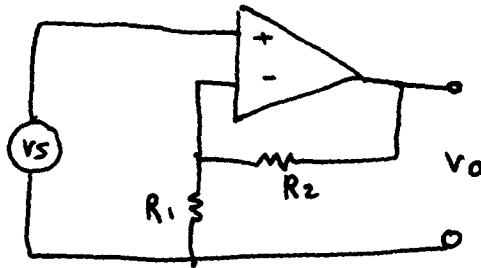
inverting amplifier



$$V_s + 0 + 0 \frac{V_o}{R_2}$$

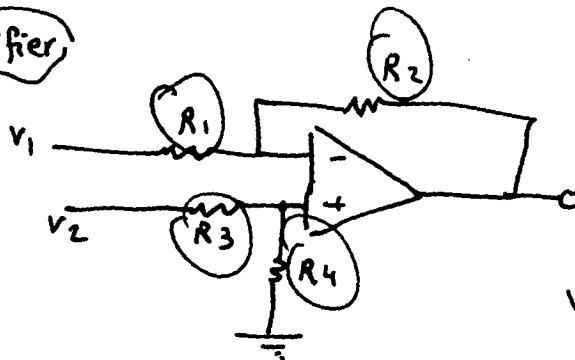
$$V_o = -\frac{R_2}{R_1} V_s$$

noninverting amplifier



$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_s$$

Differential amplifier

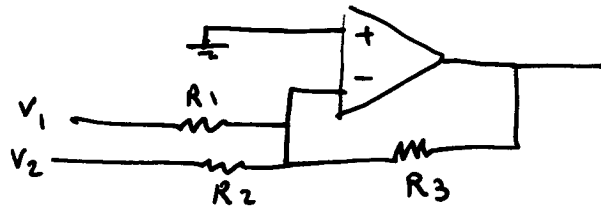


$$V_o = \frac{R_2}{R_1} \left(1 + \frac{R_1}{R_2}\right) \frac{R_4}{R_3 + R_4} v_2 - \frac{R_2}{R_1} v_1$$

if $R_4 = R_2$
 $R_3 = R_1$

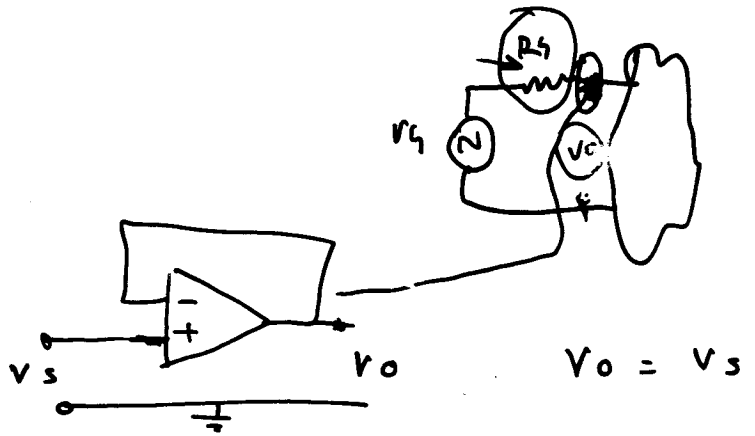
$$V_o = \frac{R_2}{R_1} (v_2 - v_1)$$

inverting adder



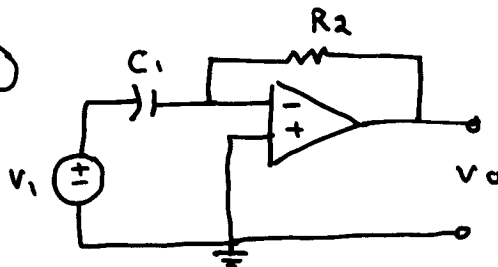
$$V_{out} = -\frac{R_3}{R_1} V_1 - \frac{R_3}{R_2} V_2$$

voltage follower



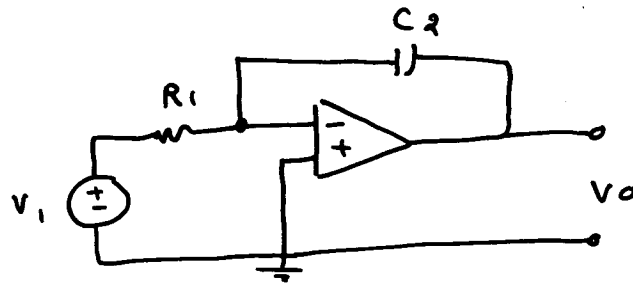
$$V_o = V_s$$

Differentiator



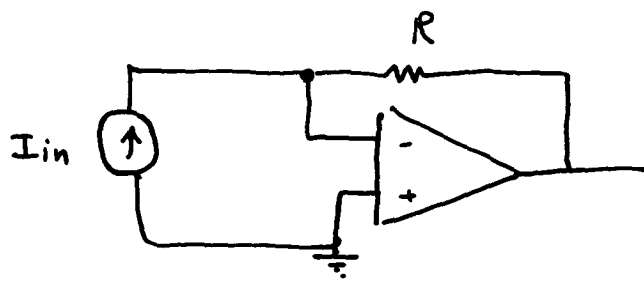
$$V_o = -R_2 C_1 \frac{dV_i(t)}{dt}$$

Integrator



$$V_o(t) = -\frac{1}{R_1 C_2} \int_0^t V_i(x) dx$$

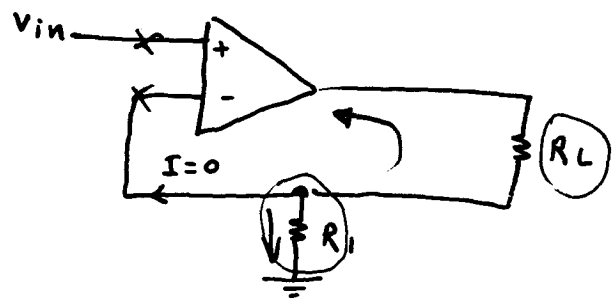
Current to voltage



$$V_{out} = -I_{in} \cdot R$$

voltage to current

R_1 is fixed $\approx 10k$
we need constant current to R_L

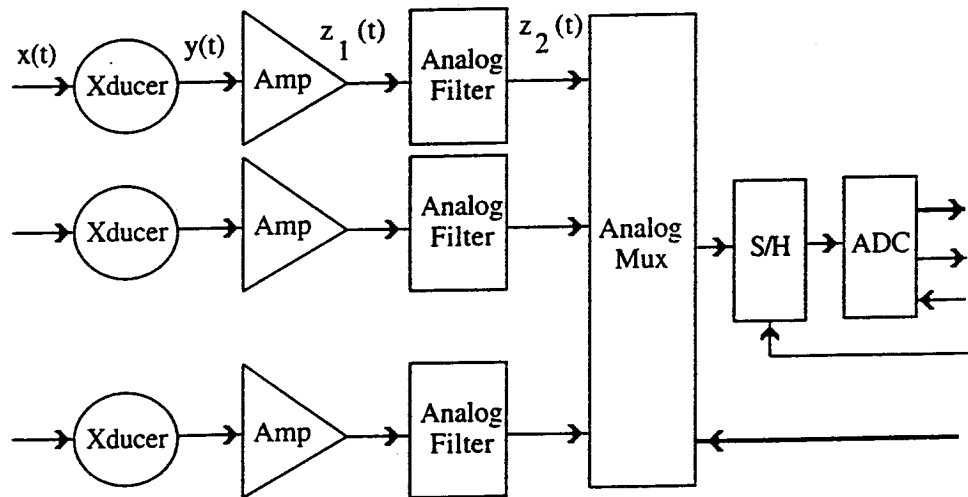


$$I_{out} = \frac{V_{in}}{R_1}$$

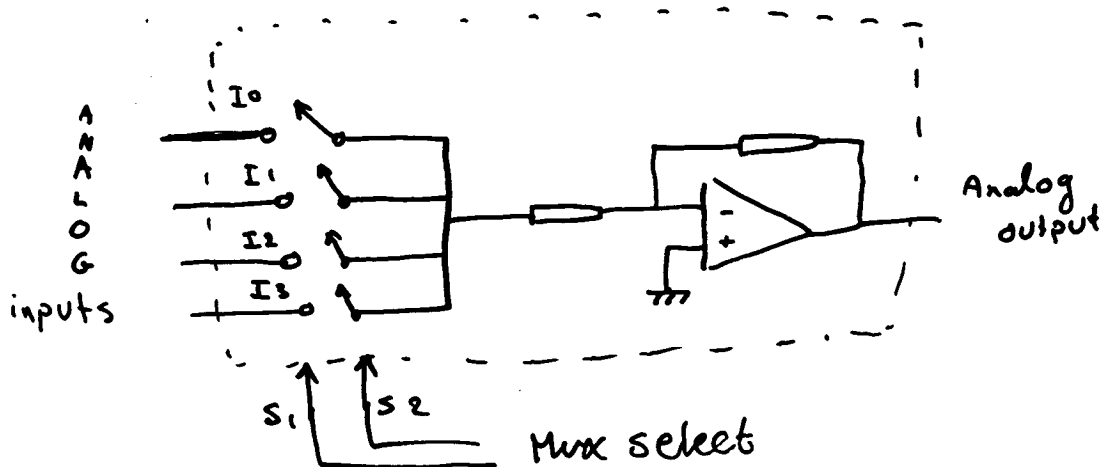
Analog MUX

when several signals need to be converted an analog MUX is used

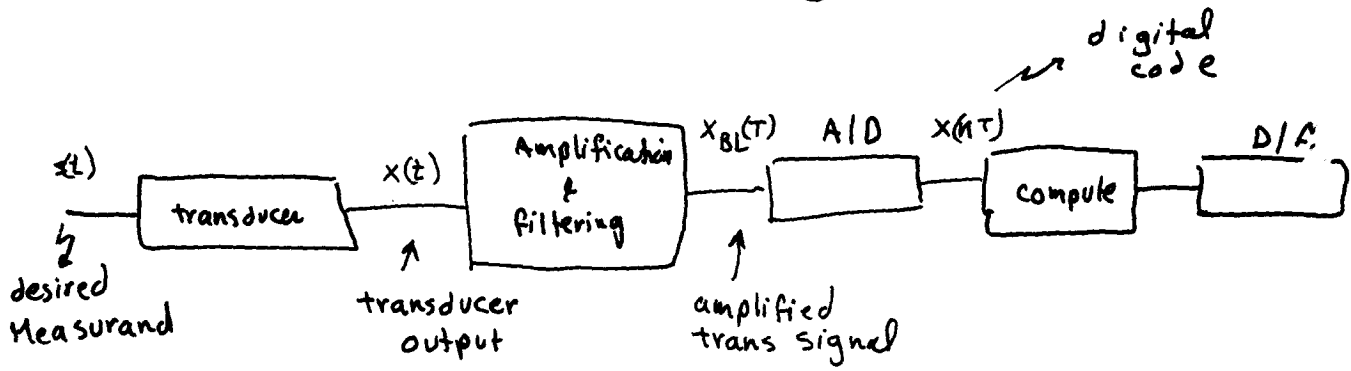
Figure 12.21
Block diagram showing how an analog multiplexer is used to sample multiple signals.



Analog signal MUX



Digital to analog converters



① The key element that allows interfacing between analog transducer & digital system is A/D

② ADC accept Band limited analog input signal & convert this signal to digital code

↓
Output code represents the strength of the input signal at the time of conversion

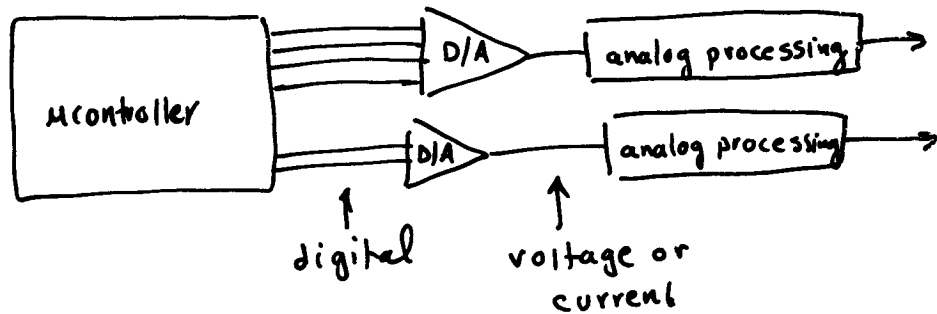
In many cases it is necessary to convert this processed signal to an analog or continuous output signal

↓
DAC

Example of a system that requires ADC & DAC

- ① control applications
- ② Music $\xrightarrow{\text{ADC}}$ digital + delay & attenuated digitally \Rightarrow simulated echo signal

Digital to Analog converters



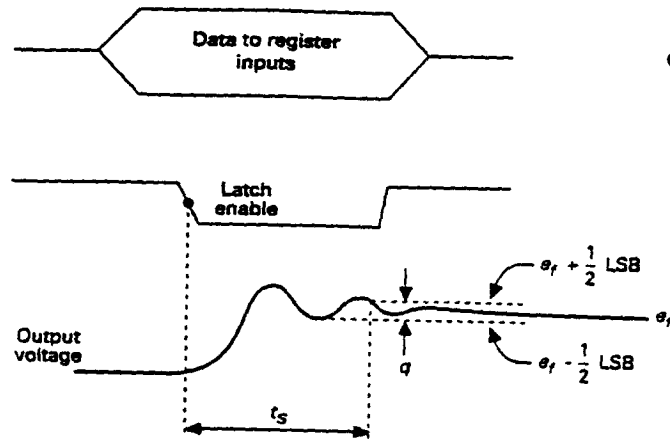
- D/A precision is the number of distinguishable D/A outputs (e.g. 256 alternatives 8 bits)
- D/A range is the maximum and minimum D/A output (volts, amperes)
- D/A resolution is the smallest distinguishable change in output

(i.e.) resolution is the change that occurs when the digital ~~output~~ _{input} changes by 1

$$\text{Range (volts)} = \text{precision} \times \text{Resolution}$$

* performance parameters of the DAC

- ① number of bits
- ② settling time (t_s)



→ measures the interval between an abrupt change of input code and the time that the output has reached the correct analog value to within some specified accuracy

Figure 6-1 Definition of settling time.

$\pm \frac{1}{2} \text{ LSB}$

i.e when output approximates the correct value within one half of a quantum interval → settling time is completed.

Q What is the use of knowing t_s ?

Ans settling time determines the upper limit on frequency of conversion for the DAC

i.e DAC should never exceed a conversion frequency of $f_{\max} = \frac{1}{t_s}$

③ conversion factor (CF): "same as quantum interval (q)"
is defined as the change in output signal
for a unit change of input code.

Note some DACs have a fixed CF, while others
allow this parameter to be varied
by an external resistor.

* largest voltage that can be
produced by an N -bit binary DAC is

$$V_{\max} = (2^N - 1) CF$$

④ Accuracy or linearity

As the input "digital code" increases
the analog output voltage should increase
proportionally



However, due to various error sources
the increase in e_{out} may not be
perfectly linear

So, the departure from the ideal is
often specified as linearity

⑤ Resolution: often expressed in terms of the number of bits
it measures the smallest change in input
signal that is guaranteed to produce a distinguishable output
change

- D/A accuracy is $\frac{\text{actual} - \text{ideal}}{\text{ideal}}$

where ideal is referred to the national Bureau of standards

- There are two common 8-bit encoding schemes for a DAC

* unsigned: $V_{out} = V_{fs} \left(\frac{b_7}{2} + \frac{b_6}{4} + \frac{b_5}{8} + \frac{b_4}{16} + \frac{b_3}{32} + \frac{b_2}{64} + \frac{b_1}{128} + \frac{b_0}{256} \right)$

* signed 2's comp $V_{out} = V_{fs} \left(-\frac{b_7}{2} + \frac{b_6}{4} + \frac{b_5}{8} \dots \right)$

$b_7, b_6 \dots b_0$ are the 8-bit digital inputs

V_{fs} is the full scale voltage.

Design of the DAC

Two most important circuits:
 ↗ Binary weighted DAC
 ↘ Ladder DAC

Note Most popular DACs convert straight binary code to analog

BUT other codes such as

① BCD

② offset binary

③ 2's complement

} are sometimes converted

imp **One problem** that must be considered in converting a digital input code is:

"that of voltage level variation from one bit of the code to another"

Example

TTL \equiv high voltage level \rightarrow 2.4 - 5V
low " " \rightarrow 0 - 0.7V

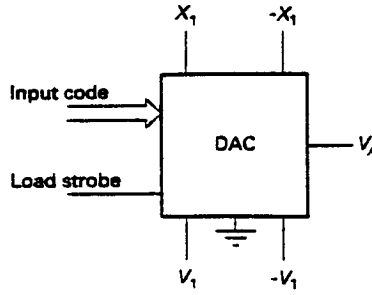
So **if** an 8-bit register drives the 8-inputs of a DAC \rightarrow all inputs may be driven with slightly different voltages (even when register contains all '1's!)

Solution:

- Use this input voltage to activate a semiconductor switch \rightarrow controls a "precise" current
- sets the digital code **into** a register that is part of the DAC. (outputs of Reg. are carefully regulated)

→ possible diagram for the DAC

IF a register is included as part of the DAC then a "load strobe" input will be present



" $V_1, -V_1$ " are power supply voltages
 " $X_1, -X_1$ " are referen voltages
 " V_A " → is analog output voltage

Figure 6-2 Block diagram of a DAC.

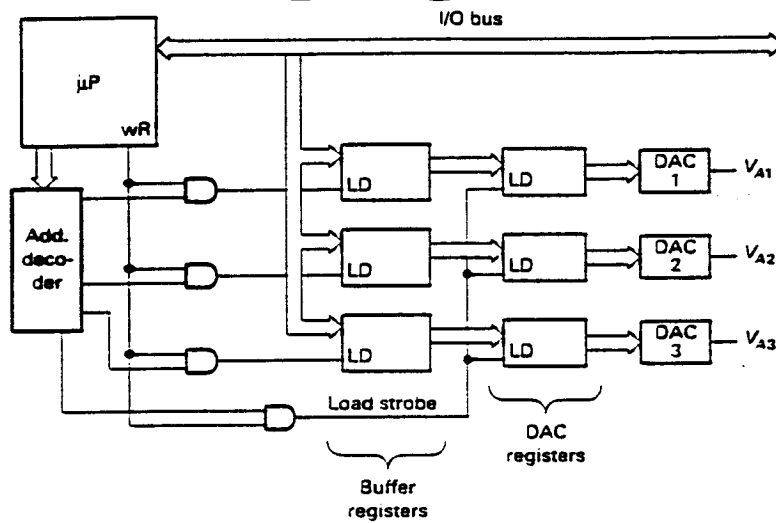
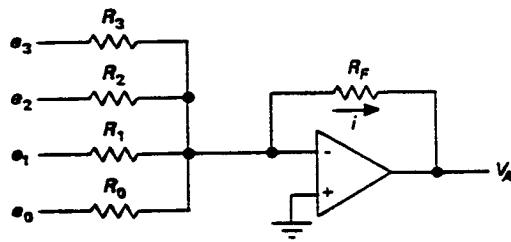


Figure 6-3 Double-buffered DACs.

* This system allows the μP to "write" to any of the three buffer registers at "any time" without changing the DAC output voltages.

→ At an appropriate time, the DAC register strobe can be applied to update the DAC registers.

Binary weighted DAC



4-bit
binary weighted

Figure 6-4 A binary-weighted DAC.

- The simplest converter is the binary weighted DAC
- This converter creates currents that are proportional to the weights of each code bit
- these currents are summed & used to produce a proportional voltage

$$V_A = - \left(\frac{e_3}{R_3} + \frac{e_2}{R_2} + \frac{e_1}{R_1} + \frac{e_0}{R_0} \right) R_F$$

- Assume input code is represented by $\left. \begin{matrix} a_3 & a_2 & a_1 & a_0 \end{matrix} \right\} a_i = "0" \text{ or } "1"$
- if voltage level associated with these two values are 0 & V_B

- if we choose the resistor values to be $R_0 = 2R_1 = 4R_2 = 8R_3$

Binary weighted $\left\{ \therefore \right.$ output voltage $V_A = \frac{-R_F}{R_0} V_B (a_3 8 + a_2 4 + a_1 2 + a_0)$

quantum interval = $CF = -\frac{R_F}{R_0} V_B$

Note CF will be set to maximum allowable value which is limited by the maximum output of OP-Amp V_{OH}

recall $V_{max} = (2^N - 1) \times CF$

so the largest conversion factor is calculated

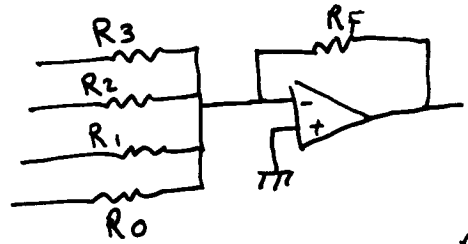
$$CF_{max} = \frac{V_{OH}}{2^N - 1}$$

imp in order to allow this input to generate an output voltage within "Active region" of amplifier

$$CF_{max} = \frac{V_{OH}}{2^N}$$

Example

The binary weighted DAC has values of $R_F = 10\text{K}$
 $R_0 = 360\text{K}$



$$R_0 = 2R_1 = 4R_2 = 8R_3$$

- (a) Calculate the conversion factor when $V_B = -8\text{V}$
(b) If V_{OM} is 8V , modify R_F to result in CF_{max}

Solution

$$(a) \quad CF = -\frac{R_F V_B}{R_0} = -\frac{(10)(-8)}{360} = 0.222$$

- so maximum output of this system

$$e_{max} = (2^N - 1) \times CF \\ = 15 \times 0.222 = 3.33\text{V}$$

- other values of resistance

$$R_1 = 180\text{K}, R_2 = 90\text{K}; R_3 = 45\text{K}$$

(b) Maximum conversion

$$CF_{max} = \frac{8}{2^4} = 0.5$$

Using this value in $CF = -\frac{R_F V_B}{R_0}$ allows

R_F to be written as

$$R_F = \frac{CF_{max} R_0}{V_B} = 22.5\text{K}\Omega$$

A practical 4-bit binary weighted DAC

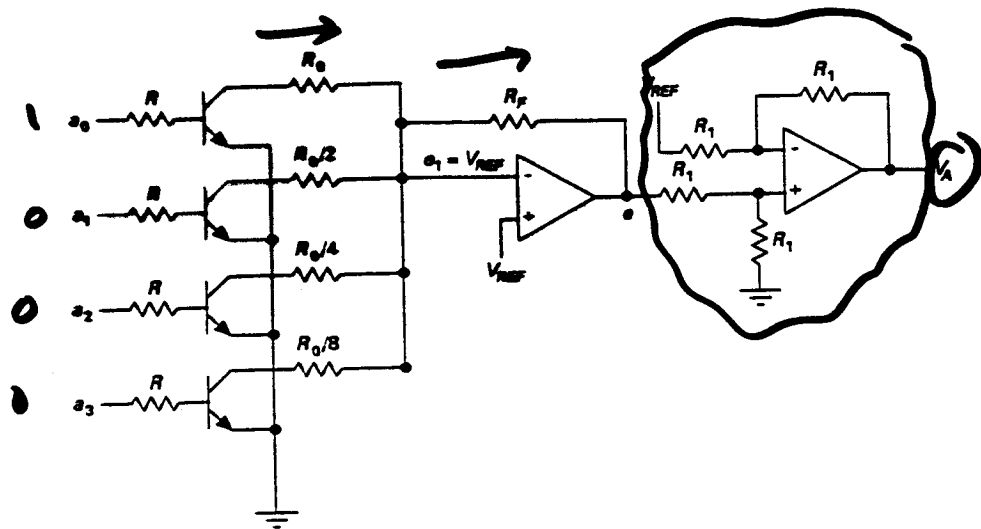


Figure 6-5 A practical 4-bit, binary-weighted DAC.

- The voltage at the inverting node is $e_1 = V_{REF}$
- when $a_0 = a_1 = a_2 = a_3 = 0 \rightarrow$ All transistors are cutoff (i.e. no current flows from inverting node)
- output voltage of first opamp = V_{REF} ✓
- when a transistor is saturated by applying a "1" to input
 a current = $\frac{V_{REF}}{R'}$ (R' is corresponding collector Res)
 flows from the inverting node
 (Assume $V_{CE(Sat)} = 0$)
 This current flows through R_F

Output of opAMP #1 $\rightarrow e = V_{REF} \left(1 + \frac{8a_3 R_F}{R_0} + \frac{4a_2 R_F}{R_0} + \frac{2a_1 R_F}{R_0} + \frac{a_0 R_F}{R} \right)$

Output of opAMP #2 $\rightarrow V_A = e - V_{REF}$

$$V_A = \frac{V_{REF} R_F}{R_0} (8a_3 + 4a_2 + 2a_1 + a_0)$$

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The binary weighted DAC is used for small word size systems (practical upper limit on $N = 6$) why?

Two major problems with this DAC are:

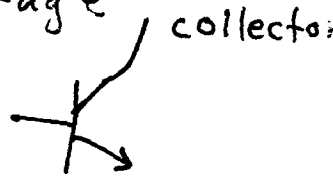
① The large resistor spread required for large word sizes
i.e. $R_0 = 2R_1 = 4R_2 = 8R_3 \dots$

✓ * problem ① with large resistance spread is difficulty of IC fabrication

* problem ② with large resistance spread is that the smallest input resistor, associated with the MSB, leads to an output that is a factor of 2^{N-1} times larger than the output for the LSB !!

Thus if the value of this resistor is inaccurate or drifts slightly due to temperature change, a change of 1 part in 2^{N-1} may lead to an output error that is larger than 1 LSB

② Speed limitation due to voltage mode switching.



parasitic capacitance at the collector of each switching transistor slows the conversion time of the DAC!!

explanation

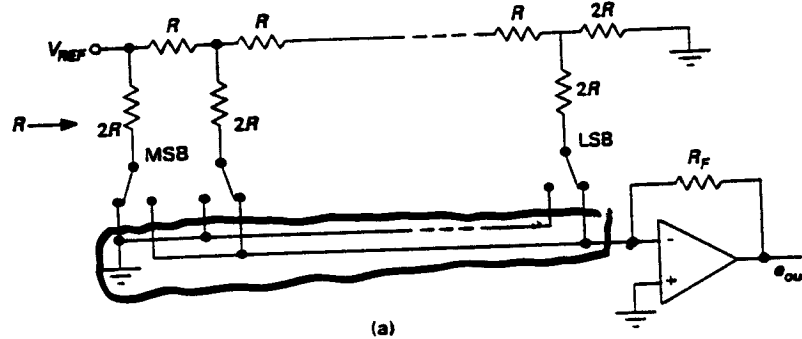
when a transistor has been saturated and then is switched off due to an input bit change \rightarrow there is a charging time constant at the collector.

\rightarrow For **LSB** this time constant is Maximum & determined by product $R_0 C$

so a 5-pF capacitance and a 20k resistance results in a time constant of 0.1 μ S

If 3 time constants are allowed for this transition \rightarrow the maximum switching speed for this bit is = 3.3 MHz

II The ladder configuration



* is used to solve the problem of resistor spread & minimize drift problem in DACs with larger value of N

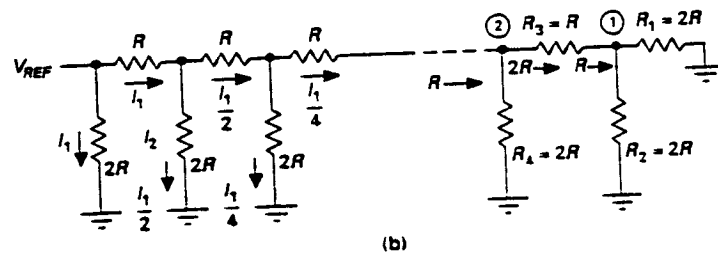


Figure 6-6 (a) A ladder DAC. (b) The equivalent ladder circuit.

IMP "virtually all IC DACs use some variation of ladder configuration"

Basic ladder configuration

- ① semiconductor switches are used to connect resistor to ground or "virtual ground"
- ② regardless of switch position the voltage at common terminal of the switch is always
- ③ This is called current switching ladder since current through the ladder resistors never changes.

Analysis

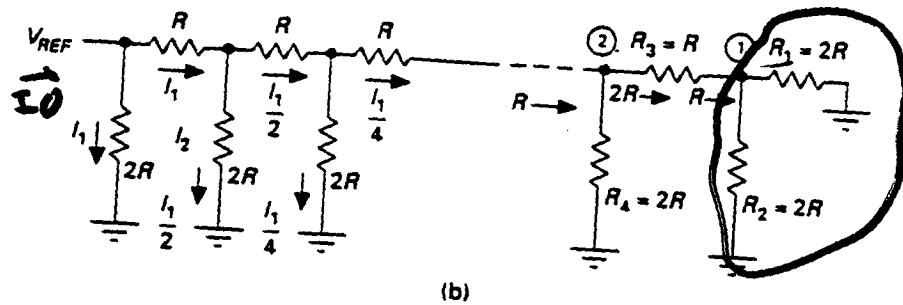


Figure 6-6 (a) A ladder DAC. (b) The equivalent ladder circuit.

(a) RHS of ladder \Rightarrow two parallel resistors R_1, R_2 of value $2R$ reduce to an equivalent resistance of R (parallel)

(b) This equivalent resistance adds in series with R_3 to present a total resistance of $2R$

(c) this equivalent resistor appears in parallel with R_4 giving a resistance of R

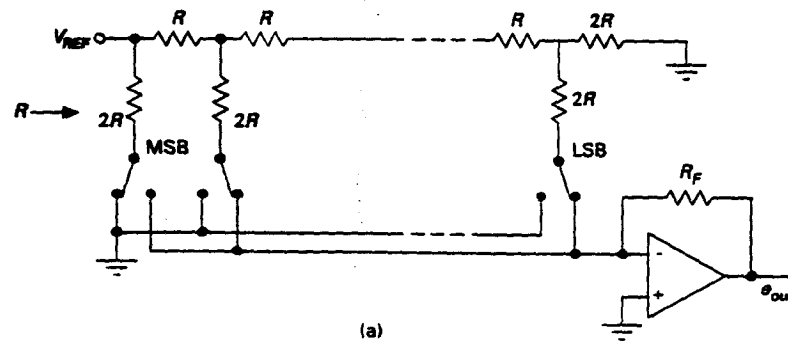
So this network is iterative $I_0 = \frac{V_{REF}}{R}$

MSB current $\leftarrow I_1 = \frac{V_{REF}}{2R}$

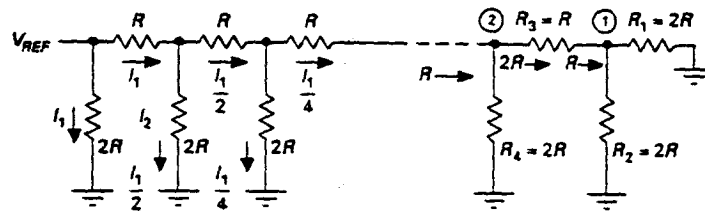
* I_1 will split in half in second node
 $I_2 = I_1/2$

* each succeeding vertical resistor has a value of current flow equal to $1/2$ that of previous

$$I_N = \frac{I_1}{2^{N-1}} = \text{LSB current}$$



(a)



(b)

Figure 6-6 (a) A ladder DAC. (b) The equivalent ladder circuit.

- ④ when a bit is '1' the switch will divert the current to the inverting input of op-amp
- ⑤ The current flows through R_F

$$e_{out} = - \frac{V_{REF} R_F}{2R} \left(a_{N-1} + \dots + \frac{a_2}{2^{N-3}} + \frac{a_1}{2^{N-2}} + \frac{a_0}{2^{N-1}} \right)$$

- ⑥ The conversion factor (CF) for ladder DAC is

$$CF = \frac{V_{REF} R_F}{2^N R}$$

Note

① The spread of resistance value for the ladder **is now** only a 2:1 spread

i.e

change in value of any single resistance **does not affect** output voltage as drastically as it can in Binary weighted DAC

⊕ IF fabricated on a chip the resistors have relatively well matched temperature coefficients (to minimize drift)

② LADDER DAC exhibits a speed advantage over binary weighted DAC

why?

Because the voltage level at the common terminal remains constant as switch position changes

⇒ Current remains constant with only path changing

So since no voltage change takes place, the **charge** on the parasitic capacitance at the input does not change

NOR do the transistors move in & out of saturation.

The Glitch problem in DACs

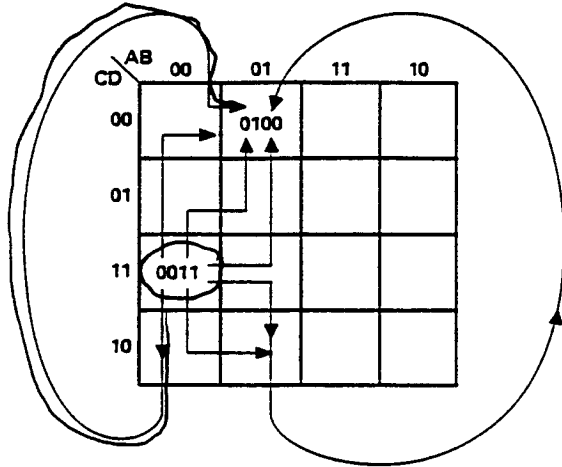


Figure 6-12 Possible paths from 0011 to 0100.

TABLE 6-4 TRANSITION PATHS FROM 0011 TO 0100

Initial state	Transient state	Transient state	Final state
0011	→ 0010	→ 0000	→ 0100
0011	→ 0001	→ 0000	→ 0100
0011	→ 0010	→ 0110	→ 0100
0011	→ 0001	→ 0101	→ 0100
0011	→ 0111	→ 0110	→ 0100
0011	→ 0111	→ 0101	→ 0100

- A significant problem occurring in DACs is that of glitching!!

* when a digital code is set into a DAC register the unequal switching times of register flip flops or the digital bit switches

can cause large transient spikes at DAC output

Because As a code changes from one value to be converted to the next value, all bits of the code do not change simultaneously.

example see Figure 6-12 & Table 6-4

Note The magnitude of the glitch depends on the significance of the bit that is changing

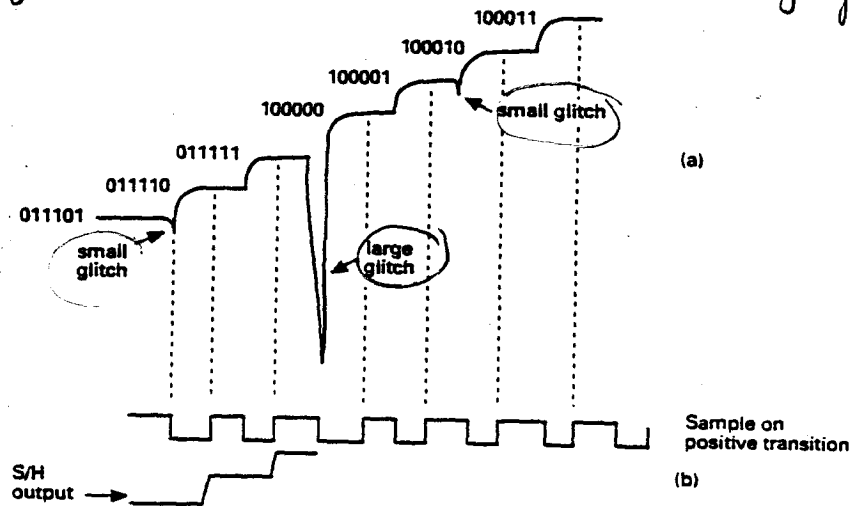


Figure 6-13 (a) DAC glitch problem. (b) S/H solution.

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Certain systems that are driven by a DAC ignore the glitches that appear at the DAC output.

Examples

① DC motors, for example cannot respond to these sharp transients due to inertia of the motor

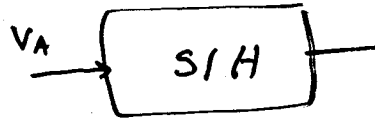
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In applications that cannot tolerate these glitches, a sample & hold circuit is typically used

→ The sample & hold circuit is driven by a signal that is out of phase with the signal that drives the input code
"In this way sampling is done after the transient has disappeared."

Sample & hold

Def: S/H is described by its name



" it samples an analog input voltage at a precise time and holds the corresponding analog value at its output "

We are interested to know

- (1) General usage of S/H
 - (2) structure (how it operates)
 - (3) when is it necessary to use S/H
 - (4) operating characteristics of S/H
- * errors associated with S/H

