

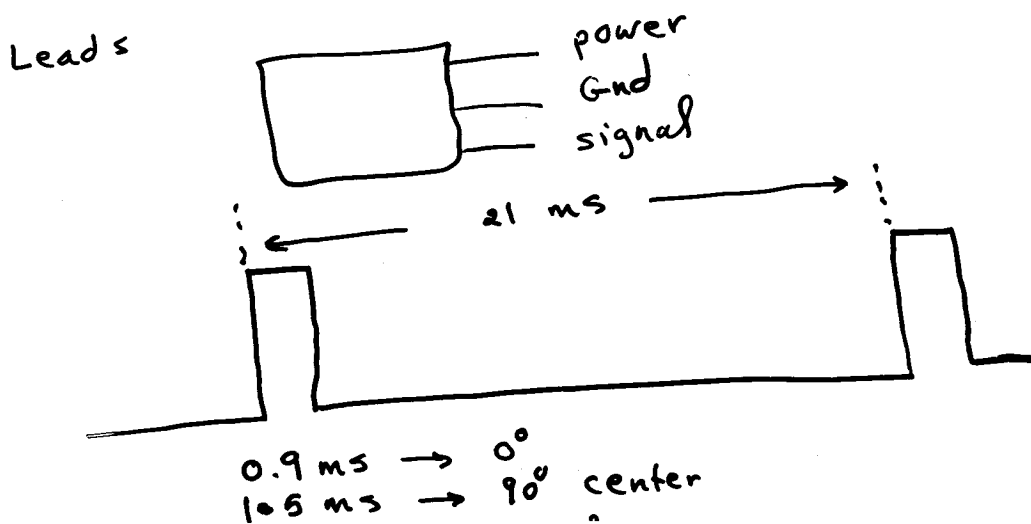
Lab # 4 Servo Motor control

objective

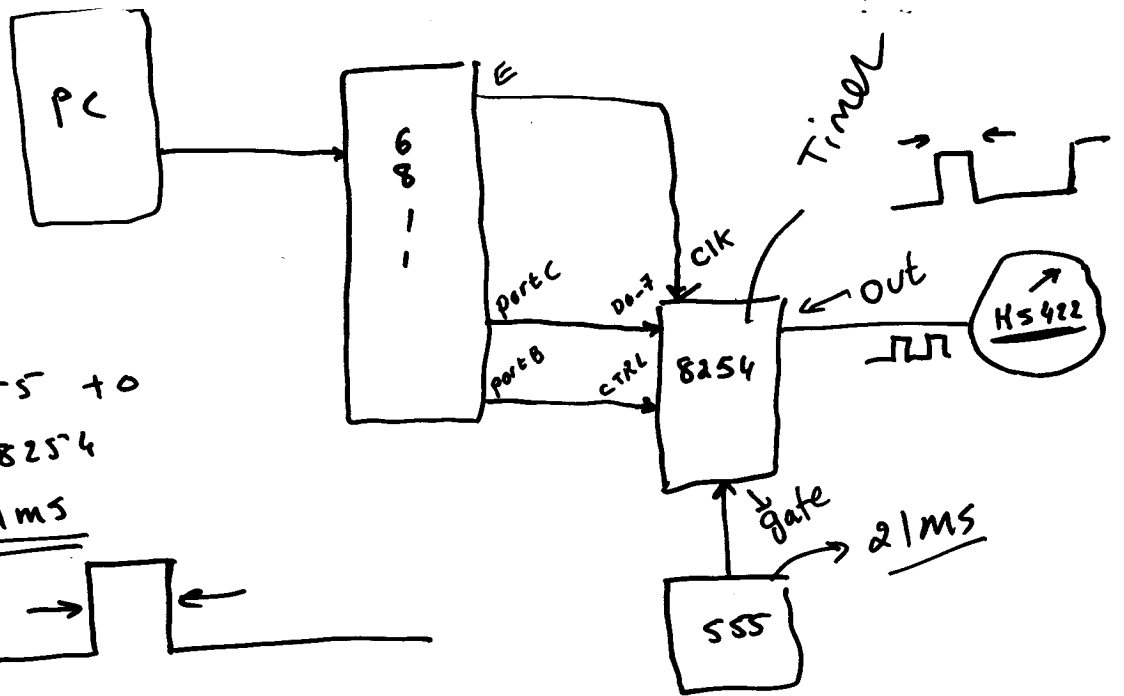
- ① controlling a servo motor by moving it to a precise position
- ② utilizing:
 - Input capture & output compare of 6811 + interrupts
 - using 555 timer + 82C54 PIT
 - How to design with constraints

servo motor

dc motor + control electronics + positional feedback potentiometer
(feedback mechanism to compare the actual position with the decoded desired position)



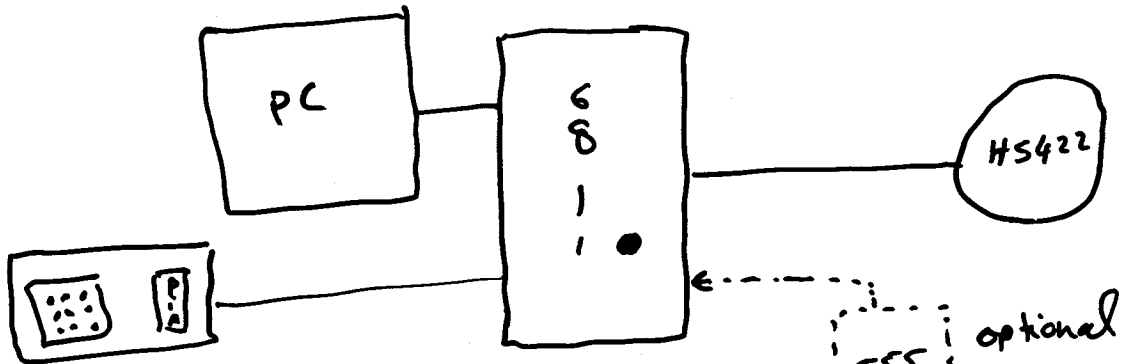
①



① Uses 555 to trigger 8254 every 2ms

② 8254 is controlled by 6811

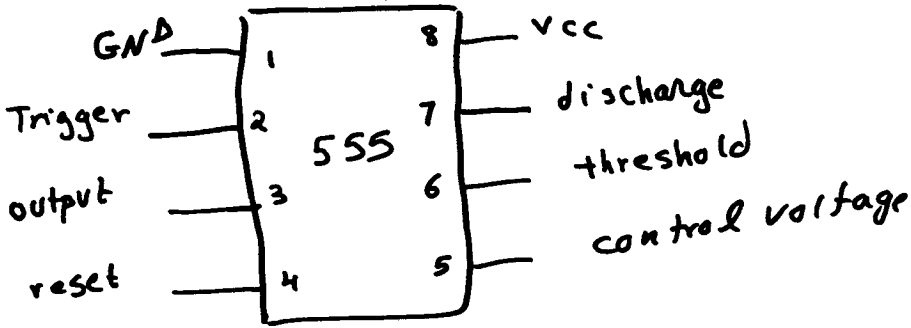
②



① either 555 can be used to trigger 6811 which will use interrupts & output compare (timing generation) to produce pulse



555 Timer → - generates accurate time delays
 - oscillator



modes

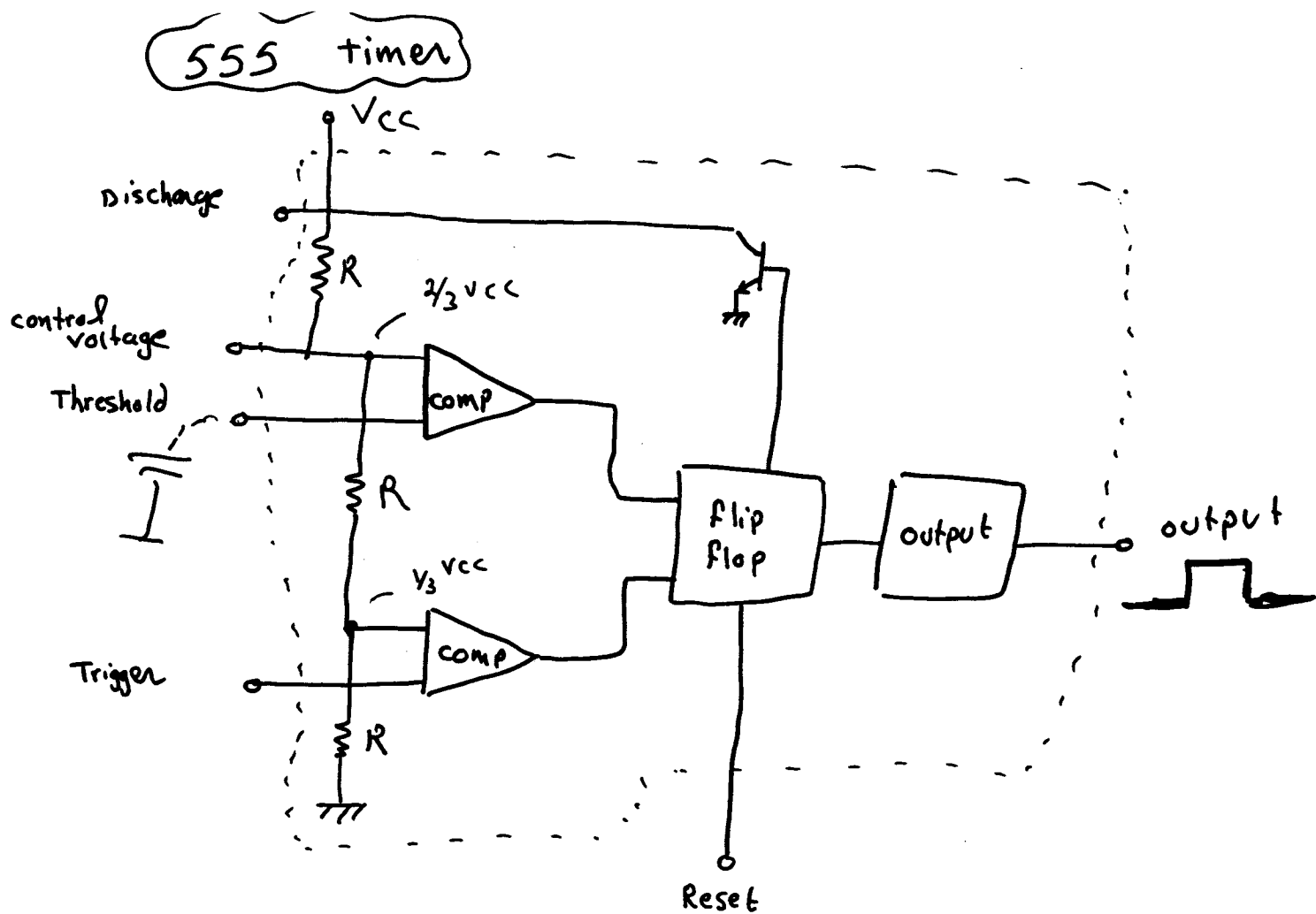
① Monostable → functions as a one-shot
 when a voltage below one third VCC is sensed by trigger comparator.
 on negative going edge the device triggers → output goes high

Requires two external components
 R
 C

② Astable → "free running mode"
 trigger is tied to threshold pin
 AT power up, capacitor is discharged holding trigger low. this triggers the timer → capacitor starts to charge
 when capacitor reaches 2/3 VCC output drops low

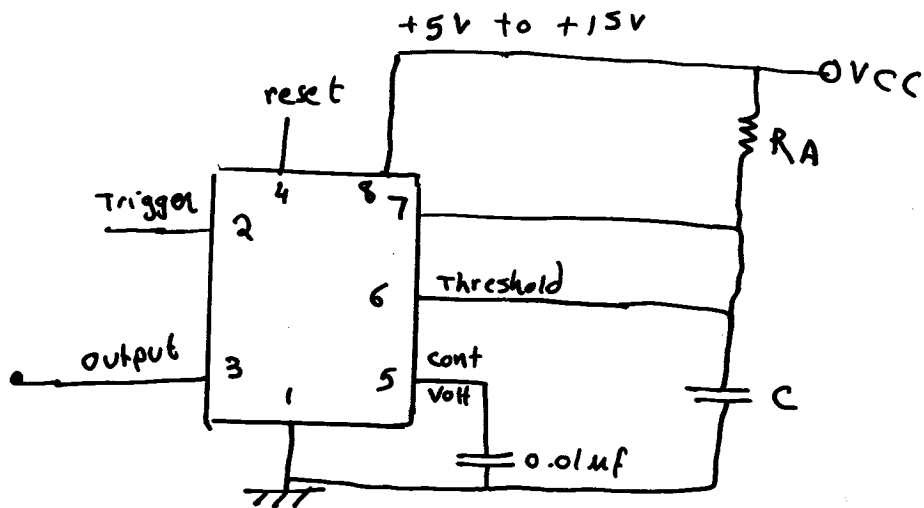


$$f = \frac{1.49}{(R_A + 2R_B)C}$$



- ① When trigger voltage is moved below $\frac{1}{3}$ of the supply
The comparator changes state and sets the f.f driving the output to a high state
 - ② The threshold pin normally monitors the capacitor voltage (not seen here!) of the RC timing network. when the capacitor voltage exceeds $\frac{2}{3}$ of the supply, the threshold comparator resets the f.f (output = low)
- * When output is in low state \rightarrow discharge transistor is on thereby discharging the external timing capacitor

Monostable operation



- external cap is initially held discharged by transistor
- Upon application of a negative trigger pulse $< \frac{1}{3} V_{CC}$ to (trigger pin) the flip flop is set \rightarrow (drives output high)
- voltage across capacitor increases exponentially $\approx \frac{2}{3} V_{CC}$ Comparator resets flip flop which in turn discharge capacitor & drives (the output Low)

e.g time = 0.1 ms

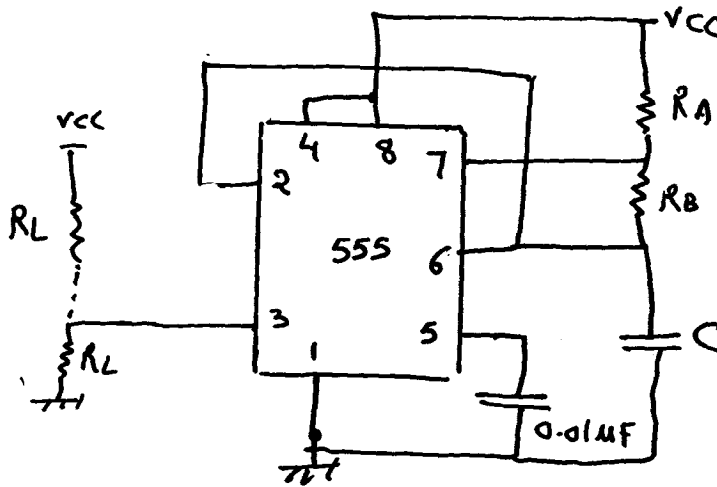
$R_A = 9.1 \text{ k}\Omega$

$C = 0.01 \mu\text{F}$

*

Astable operation

Note pin(2 Trigger) & pin(6 threshold) are tied together & 555 will trigger itself (free runs as multivibrator)



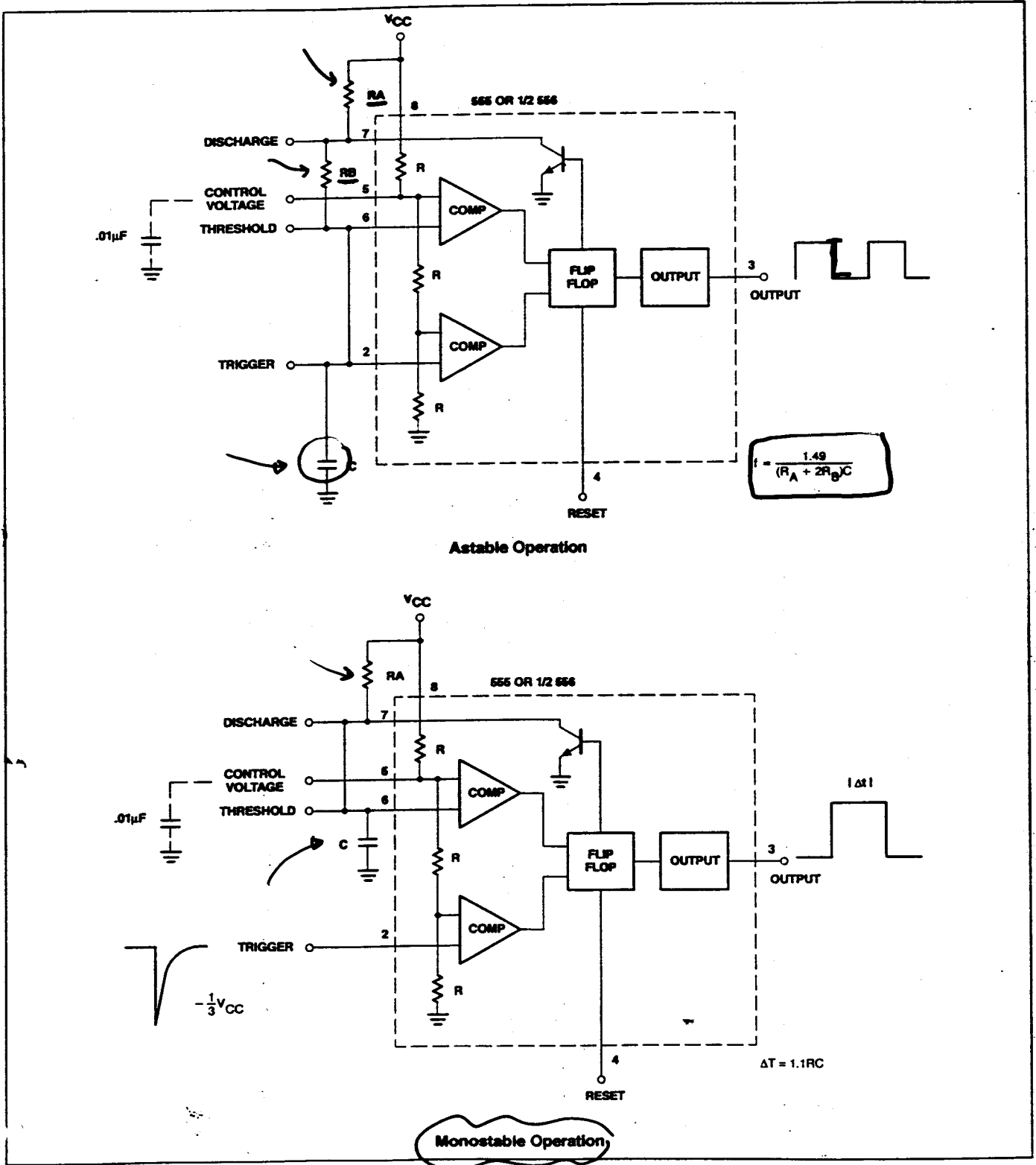
* external capacitor charges through $R_A + R_B$
& discharges through R_B

* so duty cycle may be precisely set by the ratio of these resistors.

Timer

NE/SA/SE555/SE555C

TYPICAL APPLICATIONS



- By proper selection of external components, oscillating frequencies from one cycle per half hour ! to 500 kHz can be realized.
- Duty cycles can be adjusted from less than 1% to 99% over the frequency spectrum.

For astable operation :

The charge time is given by (output high)

$$t_1 = 0.693 (R_A + R_B) C$$

Discharge time (output low)

$$t_2 = 0.693 (R_B) C$$

Thus total time period is :

$$T = t_1 + t_2 = 0.693 (R_A + 2R_B) C$$

frequency of oscillation $f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$

Pin Description (Continued)

SYMBOL	DIP PIN NUMBER	TYPE	DEFINITION															
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.															
A0, A1	19 - 20	I	ADDRESS: Select inputs for one of the three counters or Control Word Register for read/write operations. Normally connected to the system address bus. <table border="1" data-bbox="527 340 1068 527"> <thead> <tr> <th>A1</th> <th>A0</th> <th>SELECTS</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Counter 0</td> </tr> <tr> <td>0</td> <td>1</td> <td>Counter 1</td> </tr> <tr> <td>1</td> <td>0</td> <td>Counter 2</td> </tr> <tr> <td>1</td> <td>1</td> <td>Control Word Register</td> </tr> </tbody> </table>	A1	A0	SELECTS	0	0	Counter 0	0	1	Counter 1	1	0	Counter 2	1	1	Control Word Register
A1	A0	SELECTS																
0	0	Counter 0																
0	1	Counter 1																
1	0	Counter 2																
1	1	Control Word Register																
CS	21	I	CHIP SELECT: A low on this input enables the 82C54 to respond to RD and WR signals. RD and WR are ignored otherwise.															
RD	22	I	READ: This input is low during CPU read operations.															
WR	23	I	WRITE: This input is low during CPU write operations.															
V _{CC}	24		V _{CC} : The +5V power supply pin. A 0.1μF capacitor between pins VCC and GND is recommended for decoupling.															

Functional Description**General**

The 82C54 is a programmable interval timer/counter designed for use with microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other computer/timer functions common to microcomputers which can be implemented with the 82C54 are:

- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Data Bus Buffer

This three-state, bi-directional, 8-bit buffer is used to interface the 82C54 to the system bus (see Figure 1).

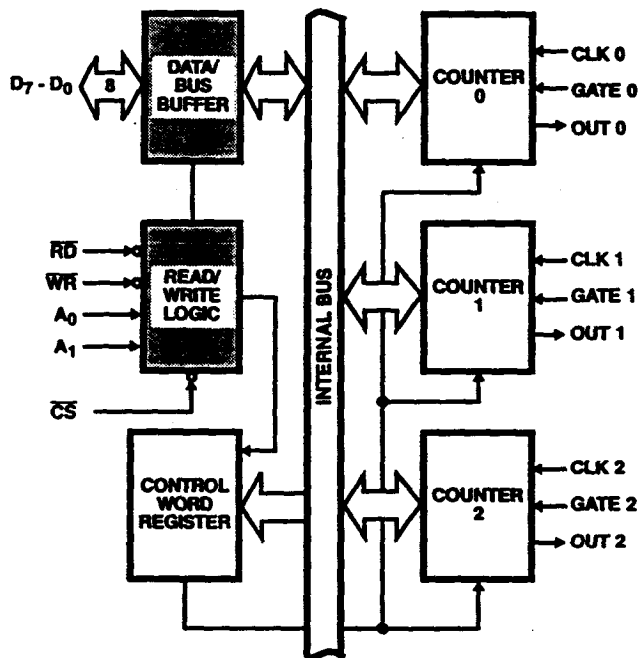


FIGURE 1. DATA BUS BUFFER AND READ/WRITE LOGIC FUNCTIONS

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 82C54. A1 and A0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the RD input tells the 82C54 that the CPU is reading one of the counters. A "low" on the WR input tells the 82C54 that the CPU is writing either a Control Word or an initial count. Both RD and WR are qualified by CS; RD and WR are ignored unless the 82C54 has been selected by holding CS low.

Control Word Register

The Control Word Register (Figure 2) is selected by the Read/Write Logic when $A_1, A_0 = 11$. If the CPU then does a write operation to the 82C54, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the Counter operation.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

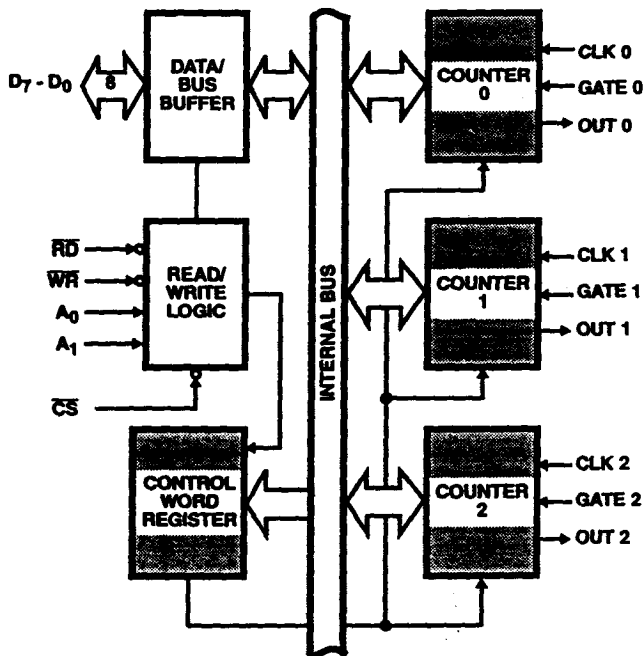


FIGURE 2. CONTROL WORD REGISTER AND COUNTER FUNCTIONS

Counter 0, Counter 1, Counter 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a signal counter is shown in Figure 3. The counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

The status register, shown in the figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labeled CE (for Counting Element). It is a 16-bit presetable synchronous down counter.

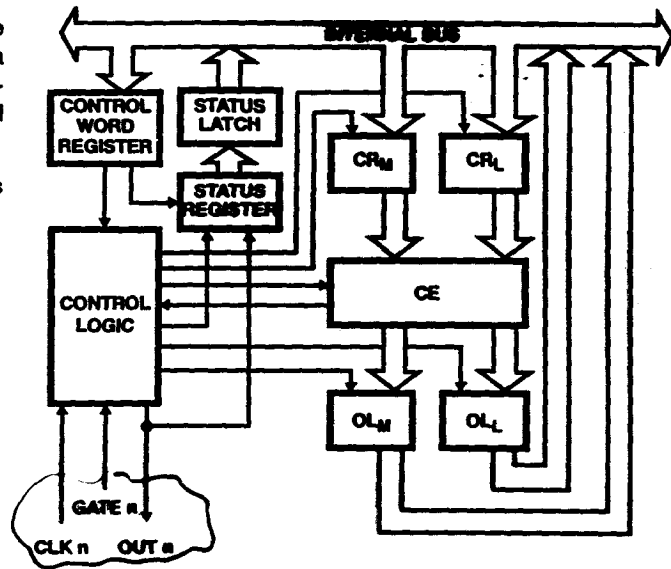


FIGURE 3. COUNTER INTERNAL BLOCK DIAGRAM

OLM and OLL are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L for "Most significant byte" and "Least significant byte", respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CRM and CRL (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CRM and CRL are cleared when the Counter is programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

82C54 System Interface

The 82C54 is treated by the system software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The \overline{CS} can be derived directly from the address bus using a linear select method or it can be connected to the output of a decoder.

Operational Description

General

After power-up, the state of the 82C54 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the 82C54

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when A1, A0 = 11. The Control Word specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A1, A0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

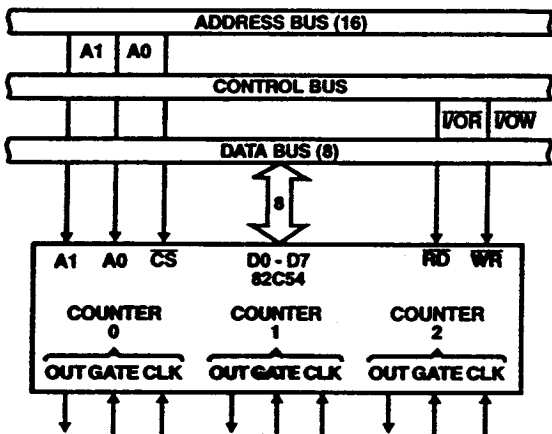


FIGURE 4. 82C54 SYSTEM INTERFACE

Write Operations

The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:

1. For Each Counter, the Control Word must be written before the initial count is written.
2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A1, A0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

Control Word Format

A1, A0 = 11; CS = 0; RD = 1; WR = 0

7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC - Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW - Read/Write

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M - Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1 *
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD - Binary Coded Decimal

0	Binary Counter 16-bit *
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

Possible Programming Sequence

	A1	A0
Control Word - Counter 0	1	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0
Control Word - Counter 1	1	1
LSB of Count - Counter 1	0	1
MSB of Count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 2	1	0

Possible Programming Sequence

	A1	A0
Control Word - Counter 0	1	1
Control Word - Counter 1	1	1
Control Word - Counter 2	1	1
LSB of Count - Counter 2	1	0

Mode 1: Hardware Retriggerable One-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggerable. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

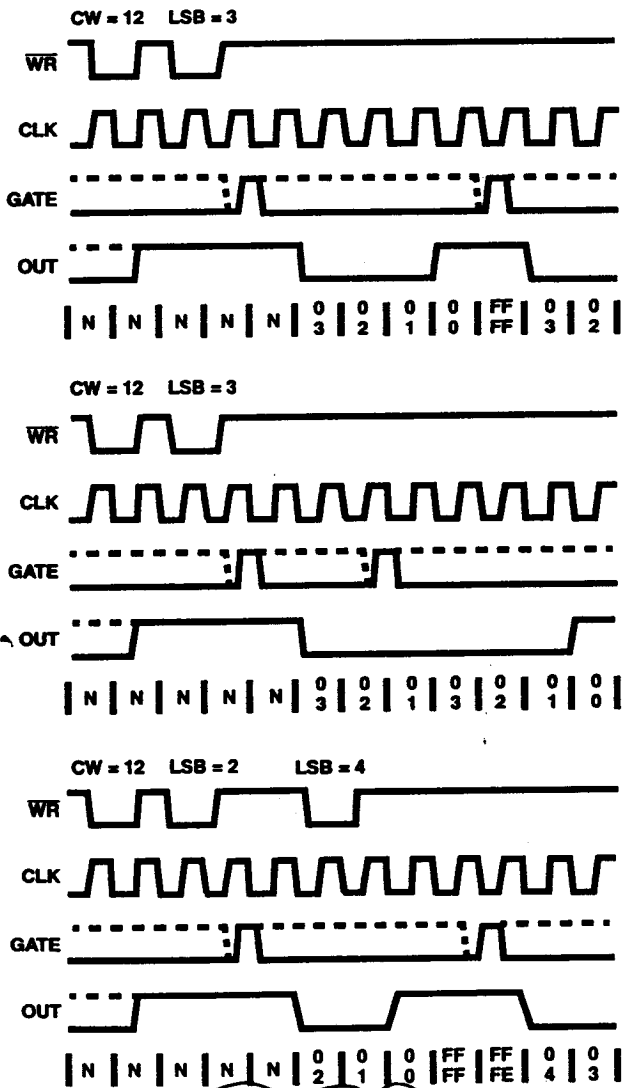


FIGURE 10. MODE 1

Mode 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock Interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of M, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the end of the current counting cycle.

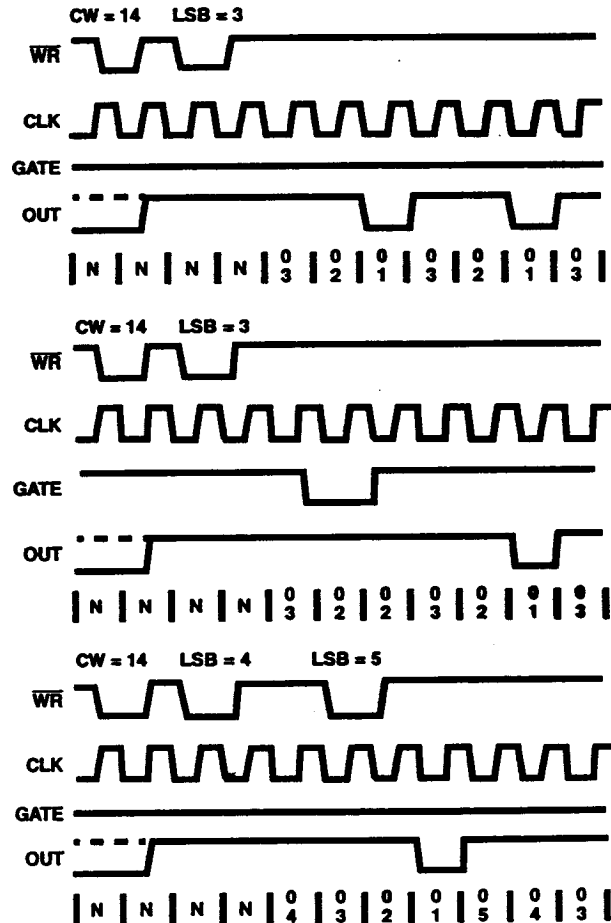


FIGURE 11. MODE 2

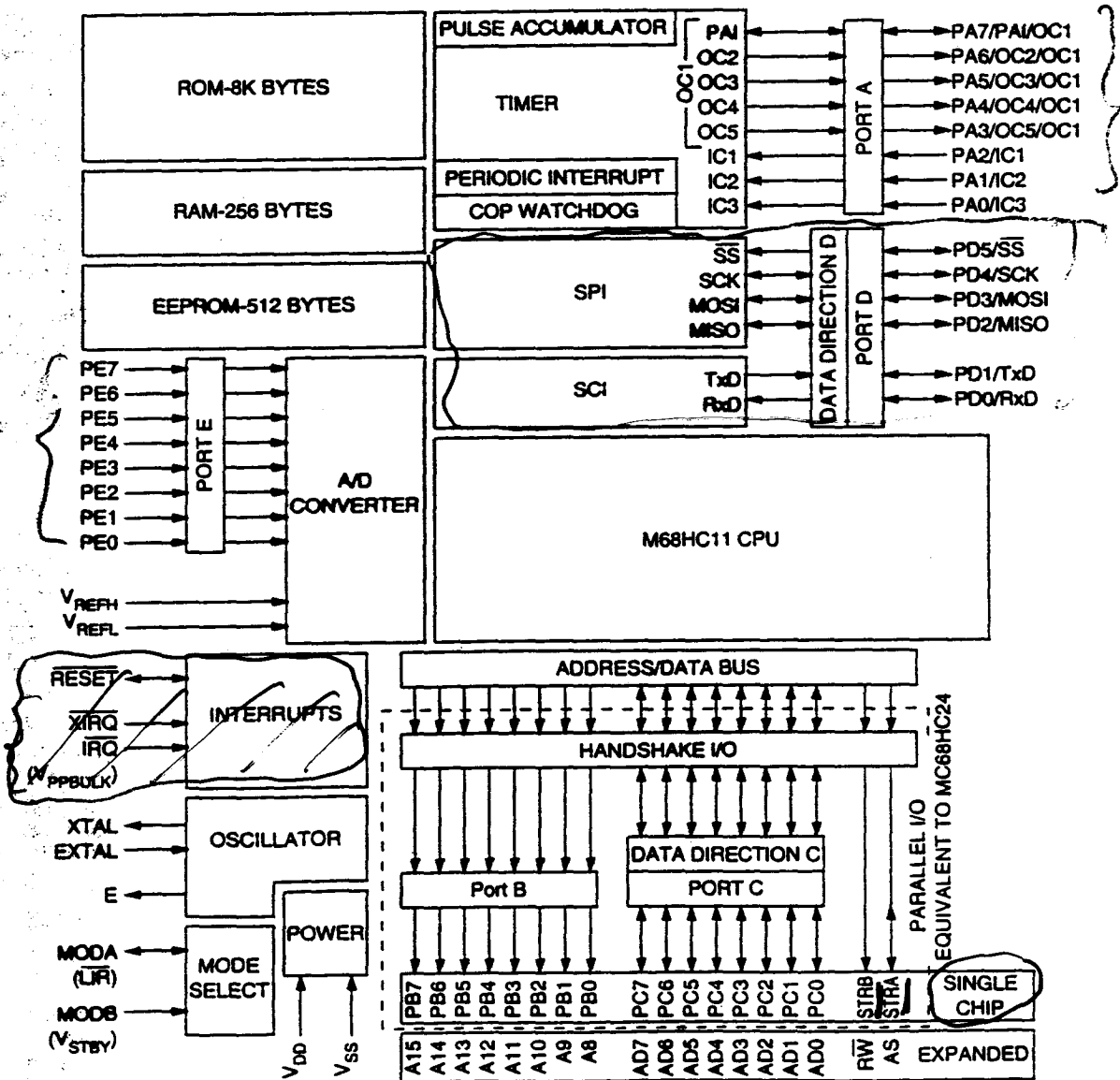


FIGURE 1.2 Internal block diagram of the MC68HC11A8 microcontroller (Courtesy of Motorola, Inc.)