

## Microcontroller Concepts

- A. What is a microcontroller?
- B. Top-down view of microcontroller systems
- C. Memory concepts
- D. Microcontroller memory map
- E. The Motorola microcontroller



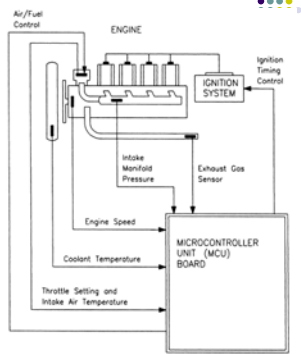
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## What is a Microcontroller?

- The microcontroller is a programmable single-chip IC that controls the operation of a system
- CPU chips with reduced computing power and with built-in memory and interface circuits



Microcontroller used to control air/fuel mixture in an automotive engine

## Top-Down View of Microcontroller Systems

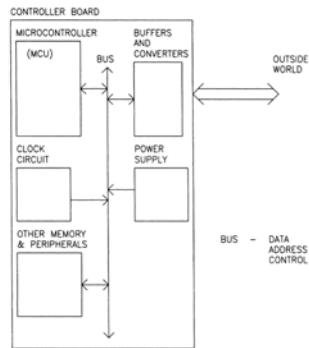
- The microcontroller system
- The microcontroller unit (MCU)
- The central processing unit (CPU)



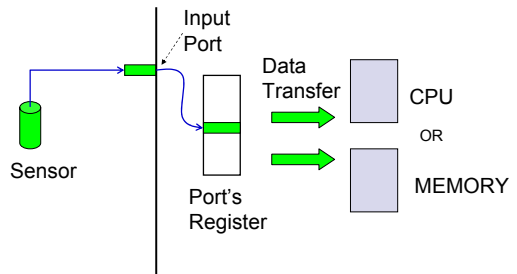
## The Microcontroller System

- Support components for the MCU

- Buffers and converters
- Bus – signals
  - data: instructions and values
  - address: location where data is stored
  - control: coordinate microcontroller operation with associated chips
- Clock circuitry
- Power circuit



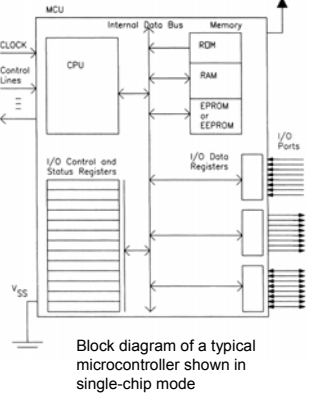
## The Microcontroller Unit (MCU) Example of an Input Operation



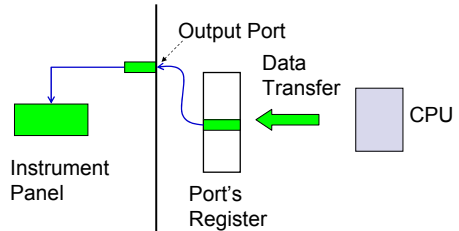
## The Microcontroller Unit (MCU)

- Microcontroller unit has 3 basic parts connected by an internal bus

- CPU
- Memory
- Registers
- I/O registers
  - data, control, status
- I/O port is a collection of I/O pins on the chip that represents a unit of data



## The Microcontroller Unit (MCU) Example of an Output Operation



## The Microcontroller Unit (MCU)

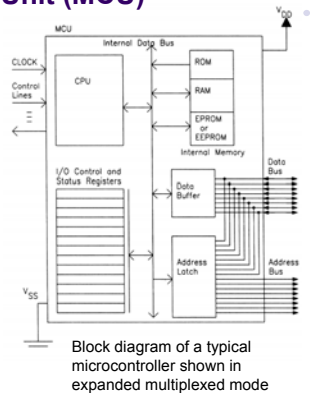


- The I/O control and data registers control and monitor the microcontroller I/O process
- Microcontrollers have internal timers
- The microcontroller uses other external pins for power and control and, if necessary, data and address lines
- RESET is a control line that is used to bring the microcontroller to an initial state
- CLOCK is also a control line

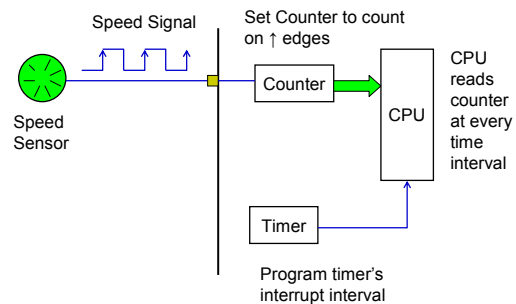
## The Microcontroller Unit (MCU) Expanded Mode



- Sometimes, a microcontroller requires more memory or I/O ports than are available in the chip mode
  - need external data and address line connections
  - some pins can be used either as I/O ports or as external data and address lines
  - set microcontroller's mode of operation



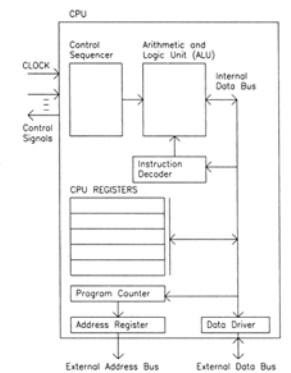
## The Microcontroller Unit (MCU) Example



## The Central Processing Unit (CPU)



- CPU executes program instructions
- Program counter (PC) is a special register that points to the instructions
- Instruction decoder tells the ALU what to do with the data
- Control sequencer manages the transfer of instruction and data bytes along the internal data bus



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- C. **Memory concepts**
- D. Microcontroller memory map
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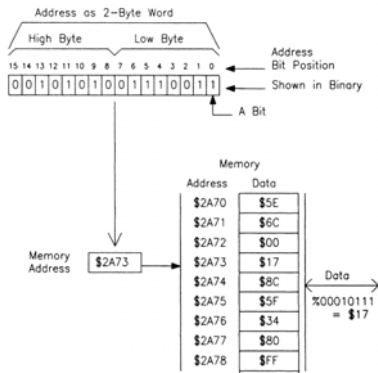
# Microcontroller Concepts

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- D. **Microcontroller memory map**
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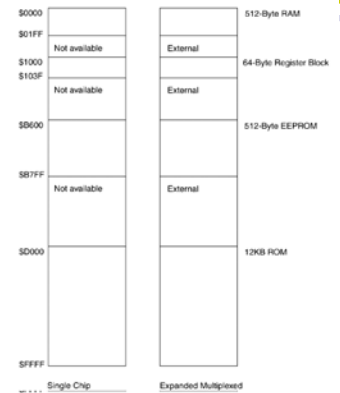
# Memory Concepts

- Numbering conventions
  - binary: %00101010
  - hexadecimal: \$2A
- Main types of memory:
  - ROM
  - RAM
  - EPROM
  - EEPROM



# Microcontroller Memory Map

- A memory map is a diagram that shows the computer's available addresses and how they are used
- The default condition is the condition of the chip, as supplied by the manufacturer
- Addressing range: 64KB for 2-byte address



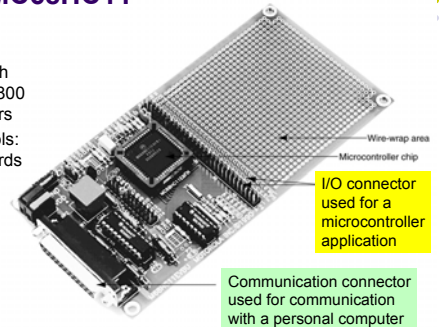
# Microcontroller Concepts

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# Motorola MC68HC11

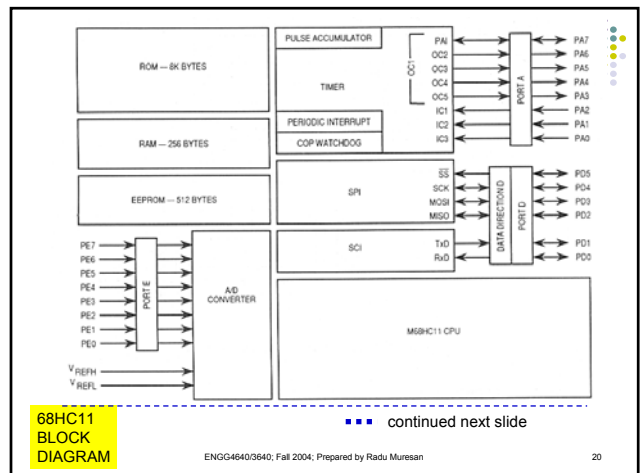
- Compatible with the Motorola 6800 microprocessors
- Prototyping tools: evaluation boards

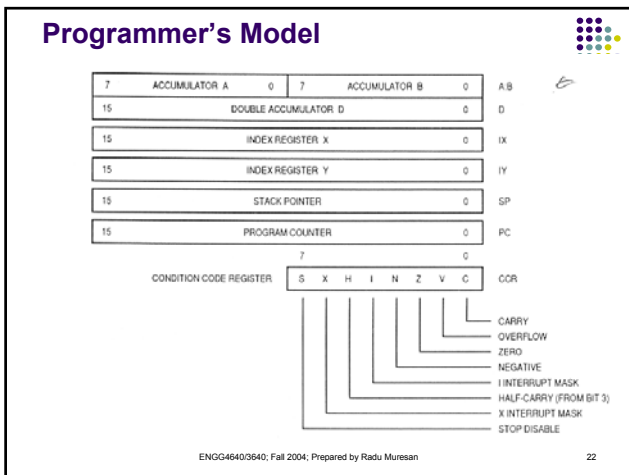
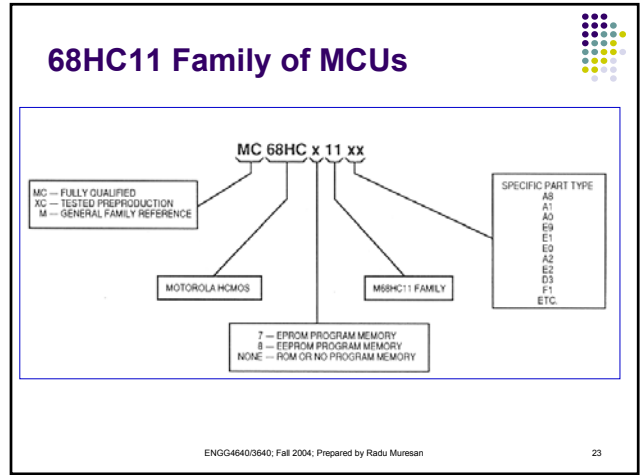
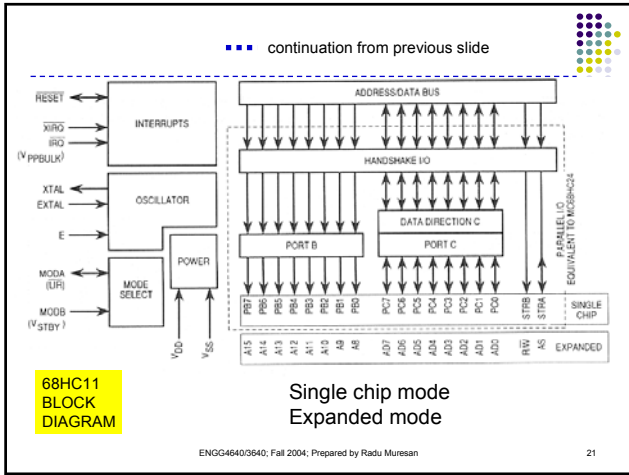


Microcontroller evaluation board. The wire-wrap area can be used for a prototype of the device being controlled.

# The Motorola Microcontroller

- Programmer's model
- Pin descriptions
- Termination of unused pins
- Configuration and modes of operation
- On-chip memory
- Resets and Interrupts





- ## Pin Descriptions
- $(V_{DD}, V_{SS}, MODB/V_{STBY}, MODA/LIR^A)$
- Power supply pins
    - $V_{DD}$  is the positive power input
    - $V_{SS}$  is the ground
  - Mode select pins
    - Mode B/standby RAM supply ( $MODB/V_{STBY}$ )
      - functions as both a mode select input pin and a standby power-supply pin
    - Mode A/load instruction register ( $MODA/LIR^A$ )
      - used to select MCU operating mode while the MCU is in reset and it operates as a diagnostic output signal while the MCU is executing instructions
- ENG04640/3640; Fall 2004; Prepared by Radu Muresan 24

## Pin Description

Inputs		Mode Description	Control Bits in HPRIO (Latched at Reset)			
MODB	MODA		RBOOT	SMOD	MDA	IRV
1	0	Normal Single Chip	0	0	0	0
1	1	Normal Expanded	0	0	1	0
0	0	Special Bootstrap	1	1	0	1
0	1	Special Test	0	1	1	1

### Hardware mode select summary

**SMOD:** special mode control bit in the highest priority interrupt (HPRIO) register

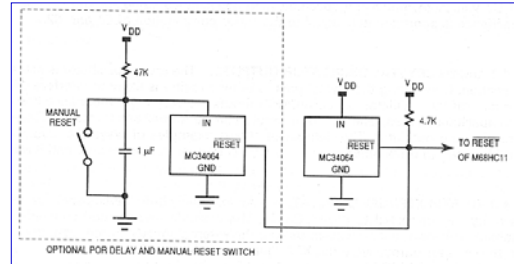
**MDA:** mode A select control bit in HPRIO

**Bootstrap** mode is the special variation of the single chip mode

**Special test** is the special variation of the expanded mode

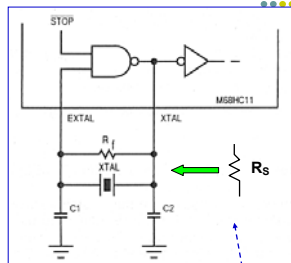
## Pin Description RESET<sup>^</sup>

- RESET<sup>^</sup> is an active-low, bidirectional control signal
- **Input:** initialize the microcontroller to a known startup state
- **Output:** indicate that an internal failure has been detected



## Pin Description (EXTAL, XTAL, E)

- Crystal oscillator and clock pins
  - E clock is the bus frequency clock output
  - E clock is free running at one-fourth the crystal frequency



Internal process  
E — Data is being addressed

High frequency crystal connection

Low frequency crystal connection

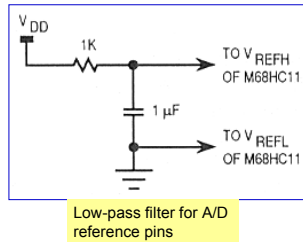
## Pin Description Interrupt pins (XIRQ<sup>^</sup>; IRQ<sup>^</sup>)

- XIRQ<sup>^</sup>: provides a mean for requesting nonmaskable interrupts after reset
  - during reset, X bit in the condition code register (CCR) is set => all interrupts are masked
  - XIRQ<sup>^</sup> is level sensitive and can be connected to a multiple-source wired-OR network
- IRQ<sup>^</sup>: provides a means for requesting asynchronous interrupts to the controller
  - IRQ<sup>^</sup> is program selectable having a choice of either level-sensitive or falling-edge-sensitive triggering

## Pin Description

### A/D Reference ( $V_{REFL}$ ; $V_{REFH}$ )

- The  $V_{REFH}$  and  $V_{REFL}$  pins provide the reference voltage for the A/D converter circuitry
  - These pins are normally connected to  $V_{DD}$  and  $V_{SS}$  through a low-pass filter network
  - There should be at least 2.5 V between  $V_{REFL}$  and  $V_{REFH}$  for full A/D accuracy



## Pin Description

### (Timer Port A Pins)

- Port A includes
  - 3 input-only pins: PA0/IC3, PA1/IC2, PA2/IC1
    - also serve as edge-sensitive timer input-capture pins
  - 4 output-only pins: PA3/OC5/OC1, PA4/OC4/OC1, PA5/OC3/OC1, PA6/OC2/OC1
    - also serve as main timer output-compare pins
    - these 4 pins can be controlled by output compare 1 (OC1) and/or another output compare
  - 1 pin that can be configured as input or output: PA7/PAI/OC1
    - general-purpose I/O; pulse-accumulator input; OC1 output pin

## Pin Description

### Port E pins (PE7-PE0)

- Port E input pins are used for general-purpose input and/or A/D analog inputs
  - the analog and digital functions of port E do not normally interfere with each other
  - digital input buffers are disabled at all times except for part of a cycle during an actual read of port E => **reduced power-supply current drains**

## Pin Description

### (Serial Port D Pins)

- Port D includes 6 general-purpose bidirectional I/O pins that can be individually configured
  - When SCI receiver is enabled => PD0/RxD becomes an input dedicated to RxD function
  - When SCI transmitter is enabled => PD1/TxD becomes an output dedicated to TxD function
  - When SPI system is enabled => PD2/MISO, PD3/MOSI, PD4/SCK, PD5/SS<sup>^</sup> become dedicated SPI functions
  - The 6 port D pins can be configured for wired-OR operation

## Pin Description (Port B and C, STRA, and STRB)

- The 18 pins are used for general purpose I/O while MCU is operating in single-chip mode
- When extended mode is used, these 18 pins become a multiplexed address/data bus with AS (address select) and R/W<sup>^</sup> (read/write) control line
- Single chip mode
  - Port B is an 8-bit output only port
  - Port C is an 8-bit bidirectional I/O port
  - Several automated handshake I/O functions are associated with ports B and C => strobe A (STRA) and strobe B (STRB) are used

## Termination of Unused Pins

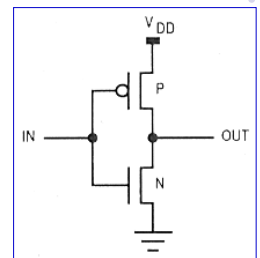
- CMOS inverter
- Avoidance of pin damage
- Zap and latchup
- Internal circuitry. Digital input-only pin
- Internal circuitry. Analog input-only pin
- Internal circuitry. Digital I/O pin
- Internal circuitry. Input/Open-Drain-Output pin
- Internal circuitry. Digital output-only pin

## Pin Description

Port	Bit	Single-Chip and Bootstrap Mode		Expanded-Multiplexed and Special Test Mode	
B	0	PB0	Output	A8	Address Output
B	1	PB1	Output	A9	Address Output
B	2	PB2	Output	A10	Address Output
B	3	PB3	Output	A11	Address Output
B	4	PB4	Output	A12	Address Output
B	5	PB5	Output	A13	Address Output
B	6	PB6	Output	A14	Address Output
B	7	PB7	Output	A15	Address Output
C	0	PC0	Input/Output	AD0	Address/Data Multiplexed
C	1	PC1	Input/Output	AD1	Address/Data Multiplexed
C	2	PC2	Input/Output	AD2	Address/Data Multiplexed
C	3	PC3	Input/Output	AD3	Address/Data Multiplexed
C	4	PC4	Input/Output	AD4	Address/Data Multiplexed
C	5	PC5	Input/Output	AD5	Address/Data Multiplexed
C	6	PC6	Input/Output	AD6	Address/Data Multiplexed
C	7	PC7	Input/Output	AD7	Address/Data Multiplexed
		STRA	Input Strobe (Edge In)	AS	Address Strobe (Out)
		STRB	Output Strobe	R/W	Read/Write Select

## CMOS Inverter

- In CMOS devices, unused pins must be terminated to assure proper operation and reliability
- The overall current drain of a CMOS device is directly proportional to the rate of switching
  - If the input is not connected it can float to a midsupply level => P and N are on => added power supply current



## Avoidance of Pin Damage



- Some inputs on the MCU (RESET<sup>A</sup>, EXTAL, MODA, MODB) cannot be left unterminated
- $V_{REFL}$  and  $V_{REFH}$  do not connect to the inputs of any CMOS gates within the MCU => no termination needed
- Types of input pins
  - A/D pins
  - input-only
  - input/output
- Unused inputs can be terminated with a pullup or pulldown resistor for each unused pin
- If a pullup or pulldown resistor is used a signal can be easily connected to the input later

## Zap and Latchup



- Zap refers to damage caused by very high-voltage static-electricity exposure
- Latchup refers to an usually catastrophic condition caused by turning on an unintentional, bipolar, silicon-controlled rectifier (SCR)
- SCR is formed by N and P regions in the layout of the IC which act as collector, base, and emitters for parasitic tr.
- Bulk resistance of silicon in the wells and substrate act as resistors in the SCR
- Application of voltages above  $V_{DD}$  or under  $V_{SS}$  => can cause latchup

## Avoidance of Pin Damage



- Any integrated circuit can be damaged or destroyed by exposure to illegal voltages or conditions
- By understanding the failure mechanisms a designer can protect against damaging conditions
- Connected to the substrate of the silicon die, the  $V_{SS}$  is the reference point from which all other voltages are measured
- $V_{DD} = 5\text{ V} \pm 10\%$

## Protective Interface Circuits

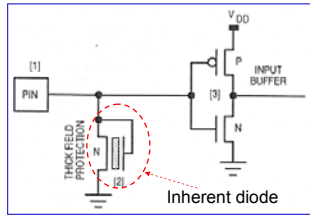


- In applications where MCU pins might be exposed to detrimental conditions, protective interfaces may be needed to protect MCU from damage
- The goals of protective interfaces are
  - prevent high currents from flowing
  - prevent illegal voltage levels at a pin
- Methods
  - low-pass filters: protect high current and voltage
  - diode clamps: high voltage protection

## Internal Circuitry. Digital Input-Only Pin



- Allowing a pin to float (or be driven) to a midsupply level can result in both the N- and P-channel devices in the input buffer simultaneously being partially on, which causes excess current and noise on the  $V_{DD}/V_{SS}$  power supply
- Port E inputs are exceptions because they are designed to be driven by analog levels

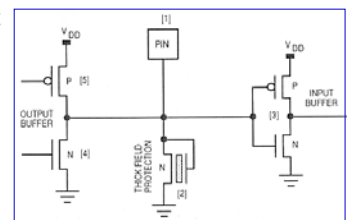


Pin current levels:  
Max: 100mA  
specified: 25mA

## Internal Circuitry. Digital I/O Pin



- The port C and port D I/O pins can be configured as open-drain-type outputs by disabling the gate signal to the P-channel device of the output buffer

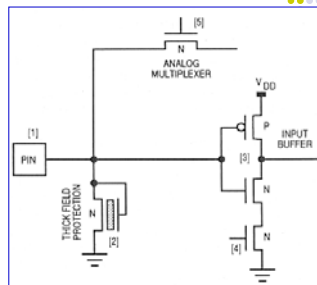


Pin current levels:  
Max: 100mA  
specified: 25mA

## Digital Circuitry. Analog Input-Only Pin



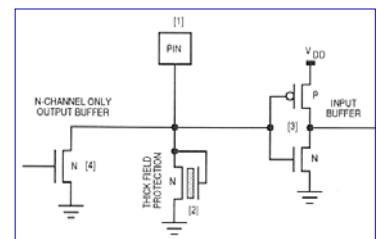
- The N-channel device [4] allows the analog input pins to be driven by intermediate levels
  - the device is only turned on for half an E-clock cycle during a digital read of port E
- The N-channel device [5] acts as an analog multiplexer



## Internal Circuitry. Input/Open-Drain-Output Pin

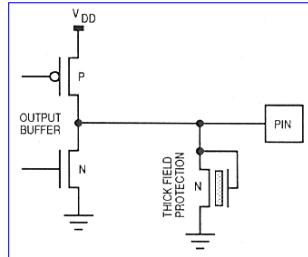


- Circuit applies for RESET<sup>^</sup> and MODA/LIR<sup>^</sup> pins



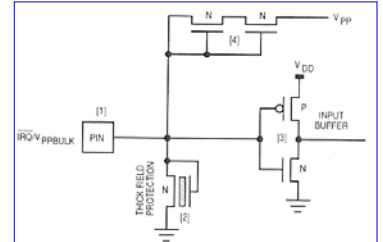
## Internal Circuitry. Digital Output-Only Pin

- Output-only pins react at illegal levels exactly like I/O pins



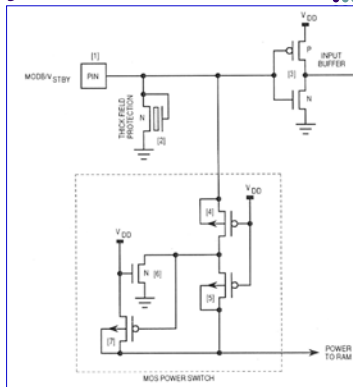
## Internal Circuitry. $IRQ^A/V_{PPBULK}$ Pin

- The  $IRQ^A$  is used as a high voltage (20V) power source during factory testing

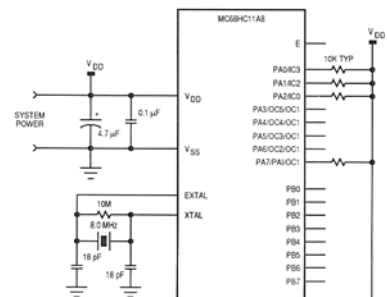


## Internal Circuitry. $MODB/V_{STBY}$ Pin

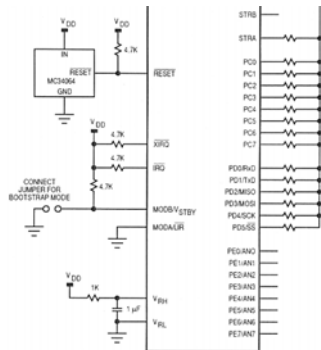
- This pin serves as a standby voltage and a mode select input
- An MOS switch automatically connects the internal RAM power supply to the higher of  $V_{DD}$  or  $V_{STBY}$



## Typical Single-Chip-Mode System Connections



## Typical Single-Chip-Mode System Connections



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## Hardware Mode Selection

Inputs		Mode Description	Control Bits in HPRI0 (Latched at Reset)			
MODB	MODA		RBOOT	SMOD	MDA	IRV
1	0	Normal Single Chip	0	0	0	0
1	1	Normal Expanded	0	0	1	0
0	0	Special Bootstrap	1	1	0	1
0	1	Special Test	0	1	1	1

- There are two fundamental modes of operation: single and expanded
- Each mode has a normal variation and a special one
- After RESET<sup>^</sup> rises the mode select pins no longer influence the MCU operating mode

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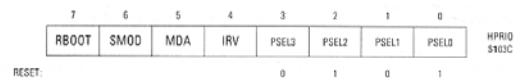
## Configuration and Modes of Operation

- Hardware mode selection
- EEPROM-based CONFIG register
- Protected control register bits
- Normal MCU operating modes
- Special MCU operating modes

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## Hardware Mode Selection Mode control bits in the HPRI0 Register

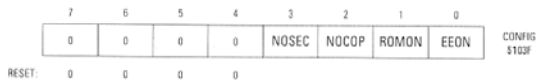


- The captured MODA and MODB levels (during the reset state) determine the logic state of the special mode (SMOD) and the mode A select (MDA) control bits in the highest priority interrupt (HPRI0) register
- SMOD and MDA control the logic circuits involved in hardware mode selection
  - RBOOT: read bootstrap ROM
    - writable only while SMOD equals one

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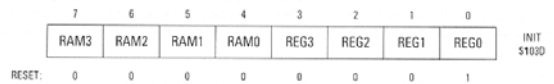
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## EEPROM-Based CONFIG Register



- CONFIG register is used to enable or disable ROM, EEPROM, the computer operating (COP) watchdog system, and, optionally, the EEPROM security feature of the MCU
- Check the MCU version for correct information about this register

## Protected Control Register Bits RAM and I/O mapping register INIT



- The INIT register allows to reposition the internal 256-byte RAM and/or 64-byte register space to any 4K page boundary in the 64K-byte memory map
- Default location after reset are:
  - RAM from \$0000-\$00FF
  - Registers from \$1000-\$103F
- Reasons for reposition capability -

## Protected Control Register Bits



- In some 68HC11 MCU versions several sensitive control registers and bits are protected against writes
  - RAM and I/O mapping register (INIT)
  - Protected control bits in the TMSK2 register
  - Protected control bits in the OPTION register
- The protect mechanism include the ability to write these bits only within the first 64 bus cycles after any reset and/or the ability to write them only one time after each reset

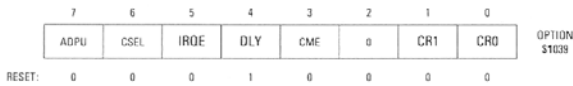
## Protected Control Register Bits TMSK2 Register



- PR1-PR0 are time-protected timer prescale select register in the timer mask register 2 (TMSK2)
- PR1-PR0 select the prescale rate for the main 16-bit, free running timer system

PR1	PR0	Prescale Factor
0	0	1
0	1	4
1	0	8
1	1	16

## Protected Control Register Bits Option register



CR1	CR0	E ÷ 12 <sup>15</sup> Divided By	Crystal Frequency		
			2 <sup>23</sup> Hz	8 MHz	4 MHz
			Nominal Time-Out		
0	0	1	15.625 ms	16.384 ms	32.768 ms
1	0	4	62.5 ms	65.536 ms	131.07 ms
1	0	16	250 ms	262.14 ms	524.29 ms
1	1	64	1 s	1.049 s	2.1 s
			Bus Frequency (E Clock)		
			2.1 MHz	2 MHz	1 MHz

- Time protected control bits on the OPTION register

## Special MCU Operating Modes



- The special mode variation are selected by having a logic zero on the MODB pin during reset
- In special mode variations, the reset and interrupt vectors are located at \$BFC0-\$BFFF

## Normal MCU Operation Modes



- MODB = 1 during reset => normal modes
  - The reset vector is fetched from \$FFFE,FFFF
  - The execution begins at the address indicated by this vector
- Normal single-chip mode operation
  - the internal 8K-byte program memory is enabled in this mode => reset vector is fetched from ROM
- Expanded mode
  - the internal 8K-byte ROM may or may not be enabled (ROMON bit in CONFIG tells this)

## ON-Chip Memory



- ROM
- RAM
- EEPROM

## On-Chip Memory



- 68HC11 includes
  - on-chip random-access memory (RAM)
  - read-only memory (ROM)
  - electrically erasable programmable ROM (EEPROM) memories
- RAM used for storage of variable and temporary information
  - 192 bytes or more
- ROM is used for storage of user program instructions and fixed data
  - 4K or more
- EEPROM is used for semipermanent information such as calibration tables, personality data, product history information, or program memory
  - 512 bytes or more

## RAM



- The on-chip RAM can be mapped to the beginning of any 4K block in the 64K-byte address space
- By default: \$0000-\$00FF
  - the first 256 locations in memory are accessible using the direct addressing mode
- The position of RAM in the 64K address space is controlled by the RAM and I/O mapping (INIT) register
- RAM standby
  - loss of primary power forces hardware standby
  - software based STOP mode is a low-power RAM standby

## ROM

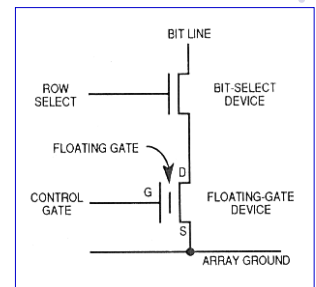


- Primary use of ROM
  - hold the user's application program instructions
- These instructions are programmed into the MCU when it is manufactured
  - they cannot be changed
- The on-chip program ROM can be disabled by an EEPROM-based control bit in the configuration control (CONFIG) register
  - an external memory is used for program instructions

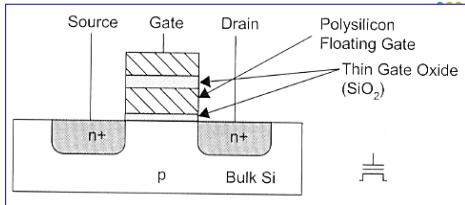
## EEPROM



- Information in EEPROM can be erased or reprogrammed under software control
  - no special power supplies are needed
- The floating-gate tr. is the storage element in the EEPROM cell



## EEPROM



- Reprogrammable nonvolatile memory has largely displaced PROMs
- These memories, including EPROM, EEPROM, and Flash, use a second layer of polysilicon to form a floating gate between the primary gate and the channel
  - High voltage on the upper gate => avalanche injection

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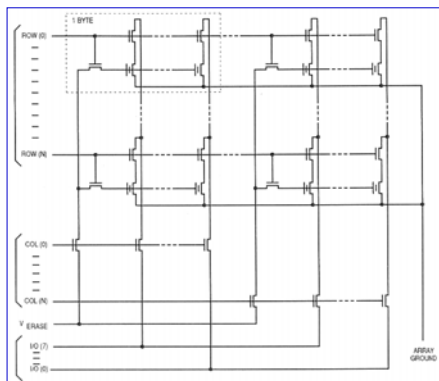
## Resets and Interrupts

- Initial conditions established during reset
- Causes of reset
- Interrupt process
- Nonmaskable interrupts
- Maskable interrupts
- Interrupt request
- Interrupts from internal peripheral subsystems

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## EEPROM



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## Initial Conditions Established During Reset

- Reset is used to force the MCU to assume a set of initial conditions and to begin executing instructions from a predetermined starting address
- Internal registers and control bits are forced to an initial state
- These initial states, in turn control on-chip peripheral systems to force them to known start-up-states

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## Initial Conditions Established During Reset



- **CPU:** after reset, the CPU fetches the restart vector from locations \$FFFE, FFFF
- The stack pointer and other CPU registers are indeterminate
- X and I interrupt mask bits in CCR are set
- S bit in CCR is set to disable the STOP mode
- **Memory map:**
- RAM and I/O mapping (INIT) register is initialized to \$01 =>
  - RAM: \$0000-\$00FF
  - Control registers: \$1000-\$103F
- ROM and EEPROM may or may not be present
  - CONFIG register

## Initial Conditions Established During Reset



- **Real-Time Interrupt**
- real-time interrupt flag is cleared
- automatic hardware interrupts are masked
- rate control bits are cleared
- **Pulse Accumulator**
- pulse accumulator is disabled => pulse accumulator (PAI) pin defaults to being a general-purpose input pin

## Initial Conditions Established During Reset



- **Parallel I/O (single)**
- STAF, STAI and HNDS control bits in PIOC register are cleared
- Port C is initialized as an input port (DDRC=\$00)
- Port B as a general purpose output port with all bits set at 0
- **Timer**
- The timer system is initialized to a count of \$0000
- The prescaler bits are cleared
- All output-compare registers are \$FFFF
- All input capture reg. are indeterminate
- OC1F is cleared

## Initial Conditions Established During Reset



- **COP watchdog**
- computer operating properly (COP) watchdog system is enabled if NOCOP control bit in the CONFIG register is clear and disabled if NOCOP is set
- **Serial communication interface (SCI)**
- SCI baud rate is indeterminate
- all transmit and receive interrupts are masked
- both the transmitter and receiver are disabled

## Initial Conditions Established During Reset



- **Serial peripheral interface (SPI)**
- SPI system is disabled
- the port pins associated with this function default to being general-purpose I/O lines
- **Analog-to-digital converter**
- A/D converter is indeterminate
- conversion complete flag is cleared
- A/D powerup (ADPU) bit is cleared => A/D system is disabled

## Causes of Reset



Reset Vector vs. Cause and MCU Mode

Cause of Reset	Normal Mode Vector	Special Test or Bootstrap Vector
POR or RESET Pin	\$FFFE,FFFF	\$BFFE,BFFF
Clock Monitor Fail	\$FFFC,FFFD	\$BFFC,BFFD
COP Watchdog Time-Out	\$FFFA,FFFB	\$BFFA,BFFB

## Causes of Reset



- **Poweron reset (POR)**
  - POR circuit triggers and initiates a reset sequence
- **COP watchdog timer reset**
  - intended to detect software processing errors
- **Clock monitor reset**
  - if no MCU clock edges are detected within an RC time delay => the clock monitor can optionally generate a system reset: RESET<sup>^</sup> is active – 4 Es
- **External reset**
  - reset can be forced by applying a low level to the RESET<sup>^</sup> pin

## Interrupt Process



- Interrupts can be enabled or disabled by mask bits (X and I) in the CCR and by the local enable mask bits in the on-chip peripheral control registers
- The instructions executed in response to an interrupt are called the interrupt service routine (ISR)
- ISR are called through the automatic hardware interrupt mechanism
- interrupt; end of current instruction; CPU registers => stack; the vector for highest priority => PC; execute ISR instructions; RTI concludes an interrupt

## Interrupt Process

- Interrupts obey a fixed hardware-priority circuit to resolve simultaneous requests
- The first 6 interrupt sources are not masked by the I bit in the CCR
  - reset; clock monitor fail; COP fail; illegal opcode; and XIRQ<sup>^</sup>
- The highest I-bit related priority input is assigned under software control (of the HPRIO register) to be connected to any one of the remaining I-bit-related interrupt sources

## Interrupt Process

**These 4 bits allow any one maskable interrupt to be elevated to the highest priority position**

PSEL3	PSEL2	PSEL1	PSEL0	Interrupt Source Promoted
0	0	0	0	Timer Overflow
0	0	0	1	Pulse Accumulator Overflow
0	0	1	0	Pulse Accumulator Input Edge
0	0	1	1	SPI Transfer Complete
0	1	0	0	SCI Serial System
0	1	0	1	Reserved (Default to IRQ)
0	1	1	0	IRQ (External Pin or Parallel I/O)
0	1	1	1	Real-Time Interrupt
1	0	0	0	Timer Input Capture 1
1	0	0	1	Timer Input Capture 2
1	0	1	0	Timer Input Capture 3
1	0	1	1	Timer Output Compare 1
1	1	0	0	Timer Output Compare 2
1	1	0	1	Timer Output Compare 3
1	1	1	0	Timer Output Compare 4
1	1	1	1	Timer Output Compare 5

## Interrupt Process

7	6	5	4	3	2	1	0	HPRIO S103C
RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	
RESET: (Refer to Table 3-1)				0	1	0	1	

## Nonmaskable Interrupt Request (XIRQ<sup>^</sup>)

- The most common use for such an interrupt is for very serious system problems such as program runaway or power failure
- Importance of X bit
  - X is set after reset => XIRQ<sup>^</sup> is inhibited
    - after software has established initial conditions the X bit may be cleared with a TAP instruction => XIRQ enabled
  - When XIRQ<sup>^</sup> occurs => CCR value is stacked with X bit cleared
    - the X bit is automatically set to inhibit nested interrupts
    - when RTI is exec. => X bit is restored to clear

## Maskable Interrupts



- After the CCR value is stacked the I bit in the CCR is set to inhibit further interrupts => there is no need for a SEI at the beginning of ISR
- The last instruction in the ISR is the RTI instruction
  - restore the registers and PC to the preinterrupt values
  - clear the I bit during normal execution of RTI => no need for CLI before RTI

## Interrupts from Internal Peripheral Subsystems



- All on-chip interrupt sources have software accessible control bits
- Each source has
  - a flag bit, which indicates service is required, and
  - an interrupt enable bit which enables the flag to generate hardware interrupt request
- The global interrupt mask I can be used to inhibit all maskable interrupts
- The interrupt status flags must be cleared after service

## Interrupt Request



- Only one IRQ pin but:
- The pulse accumulator, IC3-IC1, and STRA input pins can be used as edge-sensitive interrupt inputs
- The default configuration for IRQ is low-level-sensitive wired-OR-network
  - many interrupt sources can be accommodated to IRQ
- IRQE bit in OPTION register is used to select IRQ to be level sensitive or low-going edge sensitive
- The interrupt sources within MCU all operate as a wired-OR level-sensitive network
- In an edge-sensitive network MCU is responsible for latching a request